MT6763 LTE-A Smartphone Application Processor Technical Brief

Version:	1.0
Release date:	2017-05-15

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Document Revision History

Revision	Date	Author	Description
0.1	2016-09-30	Joseph Hou	Initial draft
0.2	2016-12-16	Joseph Hou	Update
0.3	2017-02-24	Peter Hsiao	Updated CPU frequency number.
0.4	2017-03-02	Peter Hsiao	Updated ball map.
0.5	2017-04-25	Peter Hsiao	1. Updated CPU frequency. 2. Updated Figure 2-34 ball map.
0.6	2017-05-05	Peter Hsiao	Updated package spec/modem features
1.0	2017-05-15	Peter Hsiao	1. Updated modem related descriptions 2. Updated ball map/top marking.

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

The MT6763 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A and C2K smart phone applications. The chip integrates ARM® Cortex-A53 operating up to 2.0GHz and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Octa-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

Imagination MIPS32® InterAptive, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 7, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6763 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6763 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6763

- Quad-core high performance ARM® Cortex-A53 MPCore™ operating at 2.0GHz, and the other quad-core low power ARM® Cortex-A53 MPCore™ operating at 1.5GHz
- LPDDR3 up to 4GB (single channel with 32-bit data bus width)
- LPDDR4/LPDDR4X up to 6GB (dual channels with 16-bit data bus width)
- Memory clock up to LPDDR3-1866 or LPDDR4-3733
- LTE Cat 6 (300Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 24MP@30fps
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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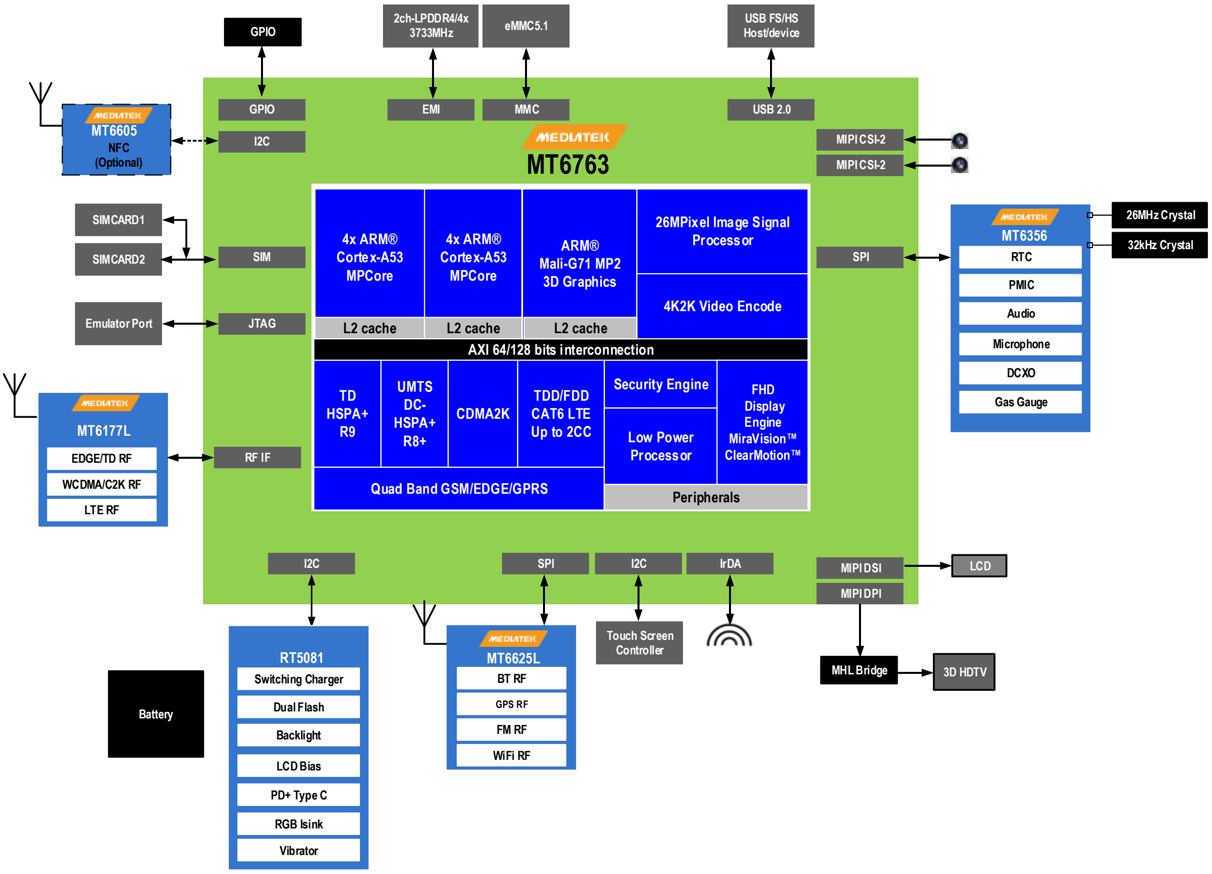

Figure 1-1. High-level MT6763 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - Supports eMMC boot
  - Supports LPDDR3
  - Supports LPDDR4/LPDDR4X

- **AP MCU subsystem**
  - Quad-core ARM® 2.0GHz Cortex-A53 MPCore™ and another quad-core ARM® 1.5GHz Cortex-A53 MPCore™
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache for each cluster
  - 512KB L2 cache for each cluster
  - DVFS technology with adaptive operating voltage from 0.6V to 1.12V

- **MD MCU subsystem**
  - Imagination MIPS32® InterAptive processor with max. 864MHz operation frequency
  - High-performance multi-core and multi-thread processor architecture (two cores and two threads)
  - 32KB L1 I-cache and 32KB L1 D-cache per core
  - 384KB SPRAM (Scratchpad memory, Two-Core's ISPRAM and DSPRAM)
  - 256KB L2 Cache (share L2 cache for two cores)
  - High-performance AXI bus Interfaces
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR3 up to 4GB (single channel with 32-bit data bus width)
  - LPDDR4/LPDDR4X up to 6GB (dual channels with 16-bit data bus width)
  - Memory clock up to LPDDR3-1866 or LPDDR4-3733
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 host mode
  - eMMC5.1
  - 2 UART for debugging and applications
  - 6 SPI masters for external devices
  - 7 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.7V/0.8V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.1V/0.6V
  - LCM interface: 1.8V

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- Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA
  - 11.8mm*11mm
  - Height: Max. 0.9mm
  - Ball count: 566 balls
  - Ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 300Mbps downlink, 50Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - 4*2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports feICIC
  - Supports MBMS
  - Uplink CoMP ability
  - Advanced Interference Cancellation
  - Transmit Atenna Selection

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements
  - Transmit Atenna Selection

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection
  - Transmit Atenna Selection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12

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- Supports SAIC (Single Antenna Interference Cancellation) technology
- VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec
- Transmit Atenna Selection

- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Simultaneous Hybrid Dual Receiver (SHDR) support
  - Supports 1x Diversity
  - Supports SRLTE
  - Transmit Atenna Selection

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1.4 Connectivity Features

MT6763 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625L. With four advanced radio technologies integrated on one chip, M6763/MT6625 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT6763 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)
- **Wi-Fi**
  - Dual-band (2.4GHz/5GHz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control
- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

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- Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Supports dual-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to FHD (1,920*1,080)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 8 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling

- **Graphics**
  - OpenGL ES 3.1/3.0/2.0/1.1 3D graphic accelerator capable of processing 140M tri/sec and 1,400M pixel/sec @ 700MHz
  - OpenCL ES 1.1 full profile

- **Image**
  - Integrated image signal processor supports 24MP@30fps
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 24M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture), [13MP + 13MP]@30fps
  - Hardware JPEG encoder: Baseline encoding with 130M pixel/sec Continuous shot with 220M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps/40Mbps
  - VP9 decoder 1080p @ 30fps/40Mbps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG2 decoder 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps
  - H.263 encoder: Simple profile D1 @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM

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- External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
- 4-band IIR compensation filter to enhance loudspeaker responses
- Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

NC		WB_RXIP		EMI0_DQ7	EMI0_DQ4		EMI0_CA2		EMI0_CA1		EMI0_DQ10		EMI1_DQ8		EMI1_DQ13		EMI1_CA3		EMI1_DQ6		MSDC0_DAT0	MSDC0_DAT2		MSDC0_DAT7	DVDD18_MSDC0	AVDD12_AP	DVSS	NC
WB_RXQN	WB_RXQP	WB_RXIN	DVSS	EMI_EXTR	EMI0_DQ6	EMI0_DQ5	EMI0_DMI0		EMI0_DMI1	EMI0_DQ14	EMI0_DQ11		EMI1_DQ10	EMI1_DQ14	EMI1_DMI1		EMI1_CA2	EMI1_DMI0	EMI1_DQ5		DVSS	MSDC0_DAT1	MSDC0_CMD	MSDC0_DAT4	MSDC0_DSL	DVSS	NC	AVDD18_AP
DVSS		DVSS		EMI0_DQS0_T	EMI0_DQ1	DVSS	EMI0_CA3	EMI0_CA4	EMI0_CS1	DVSS	EMI0_DQ8	EMI0_DQ12	EMI1_DQ9	EMI1_DQ12	EMI1_CA1	EMI1_CS1	EMI1_CA4	DVSS	EMI1_DQ4	EMI1_DQ7	EMI1_DQS0_C	DVSS	MSDC0_DAT3	MSDC0_RSTB	MSDC0_DAT5	DVSS	NC	NC
	WB_TXIN	WB_TXIP	DVSS	EMI0_DQS0_C	EMI0_DQ2	EMI0_DQ3		EMI0_CKE0	DVSS	EMI0_CK_T	EMI0_DQ15	EMI0_DQS1_C	EMI1_DQS1_T	DVSS	EMI_TP	EMI1_CK_T		EMI1_CKE1	EMI1_DQ3	EMI1_DQ1	EMI1_DQS0_T	EMI_RESET_N	MSDC0_DAT6	MSDC0_CLK		NC	DVSS	NC
WB_TXQN	WB_TXQP	DVSS	WB_CTRL5	DVSS	EMI0_DQ0	EMI0_CA5	DVSS	EMI0_CKE1	EMI0_CA0	EMI0_CK_C	EMI0_DQ9	EMI0_DQS1_T	EMI1_DQS1_C	EMI1_DQ11	EMI_TN	EMI1_CK_C	EMI1_CS0	EMI1_CA5		EMI1_DQ0	DVSS	DVSS			DVSS	NC		VQPS
		GPS_RXIP	WB_CTRL3	WB_CTRL4					EMI0_CS0	EMI0_DQ13	DVSS	DVSS	EMI1_DQ15	DVSS	DVSS	EMI1_CA0	EMI1_CKE0	EMI1_DQ2		DVSS	DVSS					DVSS	AVDD12_USB	AVDD33_USB
GPS_RXQP	GPS_RXQN	GPS_RXIN	DVSS		DVSS			AVDD18_DDR					AVDD18_DDR						AVDD18_DDR				USB_DP	CHD_DM	CHD_DP		AVDD18_USB	
	DVSS	WB_CTRL1	WB_CTRL2	DVSS	XIN_WBG			AVDD2_EMI	AVDDQ_EMI		AVDDQ_EMI	AVDD2_EMI	AVDDQ_EMI		AVDDQ_EMI	AVDD2_EMI	AVDD2_EMI	AVDDQ_EMI				DVSS	USB_DM	DVSS	DVSS	RTC32K_CK	TESTMODE	DVDD18_IOLT
AVDD18_WBG	AVDD12_WBG	WB_SCLK	WB_RSTB	WB_CTRL0	DVSS			DVSS							DVDD_TOP					DVDD_TOP		DVDD_TOP		AUD_CLK_MISO	WATCHDOG	SYSRSTB	AUD_DAT_MOSI0	
	DVDD18_IORT	ANT_SEL2	WB_SDATA	WB_SEN				DVSS	DVDD_TOP	DVDD_TOP		DVSS	DVDD_TOP	DVSS	DVSS	DVSS	DVDD_TOP_SRAM	DVSS		DVDD_MFGSYS	DVDD_MFGSYS			AUD_SYNC_MISO		AUD_SYNC_MOSI	AUD_CLK_MOSI	AUD_DAT_MOSI1
ANT_SEL0	ANT_SEL1	F2W_DATA	F2W_CLK	DVSS			DVSS		DVDD_TOP	DVDD_TOP		DVSS	DVDD_TOP	DVSS	DVSS		DVDD_TOP		DVSS	DVDD_MFGSYS			DVSS	AUD_DAT_MISO1	AUD_DAT_MISO0	PWRAP_SPI0_CSN		
CSI1B_L1P	CSI1B_L1N	CSI1B_L0P	CSI1B_L0N	CSI1A_L0N			DVSS			DVSS	DVDD_TOP_SRAM	DVSS	DVDD_TOP	DVSS	DVSS	DVSS		DVSS		DVDD_MFGSYS	DVDD_MFGSYS	DVDD_TOP	EINT12	SRCLKENA1	EINT11	PWRAP_SPI0_MI	PWRAP_SPI0_MO	PWRAP_SPI0_CK
	DVSS	CSI1A_L2N	CSI1A_L2P	CSI1A_L0P					DVSS	DVDD_MDSYS		DVDD_MDSYS	DVDD_MDSYS	DVSS	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVSS	DVSS	DVDD_MFGSYS	DVDD_MFGSYS		SRCLKENA0	DVSS			DVSS	
CSI1A_L1N	CSI1A_L1P	CSI0B_L1P	CSI0B_L1N			DVSS		DVSS	DVDD_MDSYS	DVDD_MDSYS	DVDD_TOP_SRAM	DVDD_MDSYS	DVDD_MDSYS	DVSS	DVSS	DVDD_TOP	DVDD_TOP	DVSS		DVDD_MFGSYS	DVSS		DVDD_TOP	DSI0_CKN	DSI0_D0N	DSI0_D0P	DSI0_D3N	DSI0_D3P
	CSI0A_L2P	CSI0A_L2N	CSI0B_L0P	CSI0A_L0N				DVDD_VDD_MODEM	DVDD_MDSYS	DVDD_MDSYS		DVDD_MDSYS	DVDD_MDSYS	DVSS	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVSS	DVSS	DVDD_MFGSYS	DVSS			DSI0_CKP	DSI0_D2N	DSI0_D1N		
CSI0A_L1P	CSI0A_L1N	DVSS	CSI0B_L0N	CSI0A_L0P		DVDD_TOP				DVDD_MDSYS	DVDD_TOP_SRAM	DVSS	DVDD_MDSYS	DVSS	DVDD_TOP	DVSS	DVDD_TOP	DVDD_MFG_SRAM	DVDD_MFGSYS	DVDD_MFGSYS	DVSS				DSI0_D2P	DSI0_D1P	DVSS	AVDD12_DSI
AVDD12_CSI	SDA2	SCL2	EINT10	DVSS			DVSS		DVDD_VDD_MODEM			DVSS	DVDD_VDD_MODEM	DVDD_VDD_MODEM			DVSS	DVSS			DVSS	DVDD_TOP		DPI_D6	DPI_D5	DPI_D1	DPI_D3	AVDD04_DSI
	SDA4	CAM_RST1	CAM_PDN0	DVSS	DVSS		DVSS		DVDD_VDD_MODEM		DVDD_TOP_SRAM	DVSS			DVDD_MCUSYS_SRA	DVSS	DVDD_MCUSYS					DVSS		DPI_CK	DPI_D4	DPI_D8	DPI_D2	
DVDD18_IORB	SCL4	SRCLKENAI	CAM_RST0	CAM_PDN1			DVSS		DVDD_VDD_MODEM		TN_PLLGP	TP_PLLGP	DVDD_VDD_MODEM		DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DPI_DE	DPI_VSYNC	DPI_HSYNC	DPI_D0	DPI_D7	DVDD18_IOLM
		URXD0	CAM_CLK0	CAM_CLK1		DVDD_TOP	DVSS		DVDD_VDD_MODEM			AVDD18_PLLGP		DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_MCUSYS	DVSS	DVDD_MCUSYS	MSDC1_CMD	MSDC1_DAT3		DPI_D11		
EINT9	EINT4	UTXD0		DVSS		DVSS	DVSS	DVDD_VDD_MODEM	DVDD_VDD_MODEM	DVDD_MDSYS	DVSS	AVDD12_PLLGP		DVDD_VDD_MODEM		DVSS	DVSS	DVDD_MCUSYS		DVSS	DVSS	DVDD_MCUSYS		MSDC1_DAT1	MSDC1_CLK	DPI_D10	DPI_D9	DVDD18_MSDC1
	EINT3	EINT1	EINT5	EINT7			DVDD_VDD_MODEM	DVDD_VDD_MODEM							DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS	DVDD_MCUSYS		DVDD_MCUSYS		SCL_APPM	SIM1_SCLK		SDA_APPM	MSDC1_DAT2	
KPCOL1	KPCOL0	EINT2	EINT6	EINT0		BPI_BUS4		DVSS	DVSS			DVSS	MAIN_X26M_IN			DVSS	DVDD_MCUSYS	RFIC0_BSI_D1		RFIC0_BSI_D0		INT_SIM2	BPI_ANT2	SIM1_SRST	SIM1_SIO	SIM2_SIO	MSDC1_DAT0	DVDD18_SIM
DVDD18_IORB	KPROW0	SPI_CSB	SPI_MO	SDA0	BPI_BUS1	BPI_BUS3	MISC_BSI_DO_2	MISC_BSI_DO_3		APC	DET_IP0	DET_QP0	DVSS	PRX_BB_I1	DRX_BB_I1			RFIC0_BSI_D2	RFIC0_BSI_EN	RFIC0_BSI_CK	BPI_ANT0	INT_SIM1	BPI_BUS9	DVSS	AVDD18_CPU	SIM2_SRST		
	KPROW1	SPI_MI	SPI_CLK	SCL0	BPI_BUS0	BPI_BUS2	DVDD18_IORB	MISC_BSI_CK_3	MISC_BSI_CK_2	AVDD12_MD	DET_IN0	DET_QN0		PRX_BB_Q1	DRX_BB_Q1	DRX_BB_I0	DRX_BB_Q0	DVSS		DVSS	BPI_OLAT1	BPI_BUS10		SDA3	BPI_BUS8	SIM2_SCLK	DVDD28_SIM1	DVDD28_SIM2
EINT8	PWM_A	BPI_PA_VM1	BPI_PA_VM0	BPI_OLAT0	BPI_BUS6	BPI_BUS7	CDM3P5A	MISC_BSI_CK_1	MISC_BSI_DO_1	MISC_BSI_CK_0	DVSS	TX_BB_IP0	TX_BB_IN0	DVSS	PRX_BB_I0	PRX_BB_Q0		AVDD18_MD	AVDD18_AP	AUXIN2	AUXIN3	AUXIN0		SCL3	DISP_PWM	DSI_TE	DRVBUS	DVDD28_MSDC1
NC	SCL1	SDA1		BPI_ANT1	BPI_BUS5		CDM5P5A	DVDD18_IOBR		MISC_BSI_DO_0	AVDD18_MD		TX_BB_QP0	TX_BB_QN0		DVSS		REFP		AUXIN1		AUXIN4		DVDD18_IOBL	LCM_RST		IDDIG	NC

Figure 2-1. Ball map view

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2.1.2 Pin Coordinate

Table 2-1. Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	K10	DVDD_TOP	W17	DVDD_MCUSYS
A3	WB_RXIP	K11	DVDD_TOP	W18	DVDD_MCUSYS
A5	EMI0_DQ7	K13	DVSS	W19	DVDD_MCUSYS
A6	EMI0_DQ4	K14	DVDD_TOP	W20	DVDD_MCUSYS
A8	EMI0_CA2	K15	DVSS	W21	DVDD_MCUSYS
A10	EMI0_CA1	K16	DVSS	W22	DVDD_MCUSYS
A12	EMI0_DQ10	K17	DVSS	W23	DVDD_MCUSYS
A14	EMI1_DQ8	K18	DVDD_TOP_SRAM	W24	DPI_DE
A16	EMI1_DQ13	K19	DVSS	W25	DPI_VSYNC
A18	EMI1_CA3	K21	DVDD_MFGSYS	W26	DPI_HSYNC
A20	EMI1_DQ6	K22	DVDD_MFGSYS	W27	DPI_D0
A22	MSDC0_DAT0	K25	AUD_SYNC_MISO	W28	DPI_D7
A23	MSDC0_DAT2	K27	AUD_SYNC_MOSI	W29	DVDD18_IOLM
A25	MSDC0_DAT7	K28	AUD_CLK_MOSI	Y3	URXD0
A26	DVDD18_MSDC0	K29	AUD_DAT_MOSI1	Y4	CAM_CLK0
A27	AVDD12_AP	L1	ANT_SEL0	Y5	CAM_CLK1
A28	DVSS	L2	ANT_SEL1	Y7	DVDD_TOP
B1	WB_RXQN	L3	F2W_DATA	Y8	DVSS
B2	WB_RXQP	L4	F2W_CLK	Y10	DVDD_VDD_MODEM
B3	WB_RXIN	L5	DVSS	Y13	AVDD18_PLLGP
B4	DVSS	L8	DVSS	Y15	DVSS
B5	EMI_EXTR	L10	DVDD_TOP	Y16	DVSS
B6	EMI0_DQ6	L11	DVDD_TOP	Y17	DVSS
B7	EMI0_DQ5	L13	DVSS	Y18	DVSS
B8	EMI0_DMI0	L14	DVDD_TOP	Y19	DVSS
B10	EMI0_DMI1	L15	DVSS	Y20	DVSS
B11	EMI0_DQ14	L16	DVSS	Y21	DVDD_MCUSYS
B12	EMI0_DQ11	L18	DVDD_TOP	Y22	DVSS
B14	EMI1_DQ10	L20	DVSS	Y23	DVDD_MCUSYS
B15	EMI1_DQ14	L21	DVDD_MFGSYS	Y24	MSDC1_CMD
B16	EMI1_DMI1	L24	DVSS	Y25	MSDC1_DAT3
B18	EMI1_CA2	L25	AUD_DAT_MISO1	Y27	DPI_D11
B19	EMI1_DMI0	L26	AUD_DAT_MISO0	AA1	EINT9
B20	EMI1_DQ5	L27	PWRAP_SPI0_CSN	AA2	EINT4
B22	DVSS	M1	CSI1B_L1P	AA3	UTXD0
B23	MSDC0_DAT1	M2	CSI1B_L1N	AA5	DVSS
B24	MSDC0_CMD	M3	CSI1B_L0P	AA7	DVSS
B25	MSDC0_DAT4	M4	CSI1B_L0N	AA8	DVSS
B26	MSDC0_DSL	M5	CSI1A_L0N	AA9	DVDD_VDD_MODEM
B27	DVSS	M8	DVSS	AA10	DVDD_VDD_MODEM
B28	NC	M11	DVSS	AA11	DVDD_MDSYS
B29	AVDD18_AP	M12	DVDD_TOP_SRAM	AA12	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C1	DVSS	M13	DVSS	AA13	AVDD12_PLLGP
C3	DVSS	M14	DVDD_TOP	AA15	DVDD_VDD_MODEM
C5	EMI0_DQS0_T	M15	DVSS	AA17	DVSS
C6	EMI0_DQ1	M16	DVSS	AA18	DVSS
C7	DVSS	M17	DVSS	AA19	DVDD_MCUSYS
C8	EMI0_CA3	M19	DVSS	AA21	DVSS
C9	EMI0_CA4	M21	DVDD_MFGSYS	AA22	DVSS
C10	EMI0_CS1	M22	DVDD_MFGSYS	AA23	DVDD_MCUSYS
C11	DVSS	M23	DVDD_TOP	AA25	MSDC1_DAT1
C12	EMI0_DQ8	M24	EINT12	AA26	MSDC1_CLK
C13	EMI0_DQ12	M25	SRCLKENA1	AA27	DPI_D10
C14	EMI1_DQ9	M26	EINT11	AA28	DPI_D9
C15	EMI1_DQ12	M27	PWRAP_SPI0_MI	AA29	DVDD18_MSDC1
C16	EMI1_CA1	M28	PWRAP_SPI0_MO	AB2	EINT3
C17	EMI1_CS1	M29	PWRAP_SPI0_CK	AB3	EINT1
C18	EMI1_CA4	N2	DVSS	AB4	EINT5
C19	DVSS	N3	CSI1A_L2N	AB5	EINT7
C20	EMI1_DQ4	N4	CSI1A_L2P	AB8	DVDD_VDD_MODEM
C21	EMI1_DQ7	N5	CSI1A_L0P	AB9	DVDD_VDD_MODEM
C22	EMI1_DQS0_C	N10	DVSS	AB16	DVDD_MCUSYS
C23	DVSS	N11	DVDD_MDSYS	AB17	DVDD_MCUSYS
C24	MSDC0_DAT3	N13	DVDD_MDSYS	AB18	DVDD_MCUSYS
C25	MSDC0_RSTB	N14	DVDD_MDSYS	AB19	DVDD_MCUSYS
C26	MSDC0_DAT5	N15	DVSS	AB20	DVDD_MCUSYS
C27	DVSS	N16	DVDD_TOP	AB22	DVDD_MCUSYS
C28	NC	N17	DVDD_TOP	AB24	SCL_APPM
C29	NC	N18	DVDD_TOP	AB25	SIM1_SCLK
D2	WB_TXIN	N19	DVSS	AB27	SDA_APPM
D3	WB_TXIP	N20	DVSS	AB28	MSDC1_DAT2
D4	DVSS	N21	DVDD_MFGSYS	AC1	KPCOL1
D5	EMI0_DQS0_C	N22	DVDD_MFGSYS	AC2	KPCOL0
D6	EMI0_DQ2	N24	SRCLKENA0	AC3	EINT2
D7	EMI0_DQ3	N25	DVSS	AC4	EINT6
D9	EMI0_CKE0	N28	DVSS	AC5	EINT0
D10	DVSS	P1	CSI1A_L1N	AC7	BPI_BUS4
D11	EMI0_CK_T	P2	CSI1A_L1P	AC9	DVSS
D12	EMI0_DQ15	P3	CSI0B_L1P	AC10	DVSS
D13	EMI0_DQS1_C	P4	CSI0B_L1N	AC13	DVSS
D14	EMI1_DQS1_T	P7	DVSS	AC14	MAIN_X26M_IN
D15	DVSS	P9	DVSS	AC17	DVSS
D16	EMI_TP	P10	DVDD_MDSYS	AC18	DVDD_MCUSYS
D17	EMI1_CK_T	P11	DVDD_MDSYS	AC19	RFIC0_BSI_D1
D19	EMI1_CKE1	P12	DVDD_TOP_SRAM	AC21	RFIC0_BSI_D0
D20	EMI1_DQ3	P13	DVDD_MDSYS	AC23	INT_SIM2
D21	EMI1_DQ1	P14	DVDD_MDSYS	AC24	BPI_ANT2

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D22	EMI1_DQS0_T	P15	DVSS	AC25	SIM1_SRST
D23	EMI_RESET_N	P16	DVSS	AC26	SIM1_SIO
D24	MSDC0_DAT6	P17	DVDD_TOP	AC27	SIM2_SIO
D25	MSDC0_CLK	P18	DVDD_TOP	AC28	MSDC1_DAT0
D27	NC	P19	DVSS	AC29	DVDD18_SIM
D28	DVSS	P21	DVDD_MFGSYS	AD1	DVDD18_IORB
D29	NC	P22	DVSS	AD2	KPROW0
E1	WB_TXQN	P24	DVDD_TOP	AD3	SPI_CSB
E2	WB_TXQP	P25	DSI0_CKN	AD4	SPI_MO
E3	DVSS	P26	DSI0_D0N	AD5	SDA0
E4	WB_CTRL5	P27	DSI0_D0P	AD6	BPI_BUS1
E5	DVSS	P28	DSI0_D3N	AD7	BPI_BUS3
E6	EMI0_DQ0	P29	DSI0_D3P	AD8	MISC_BSI_DO_2
E7	EMI0_CA5	R2	CSI0A_L2P	AD9	MISC_BSI_DO_3
E8	DVSS	R3	CSI0A_L2N	AD11	APC
E9	EMI0_CKE1	R4	CSI0B_L0P	AD12	DET_IP0
E10	EMI0_CA0	R5	CSI0A_L0N	AD13	DET_QP0
E11	EMI0_CK_C	R9	DVDD_VDD_MODEM	AD14	DVSS
E12	EMI0_DQ9	R10	DVDD_MDSYS	AD15	PRX_BB_I1
E13	EMI0_DQS1_T	R11	DVDD_MDSYS	AD16	DRX_BB_I1
E14	EMI1_DQS1_C	R13	DVDD_MDSYS	AD19	RFIC0_BSI_D2
E15	EMI1_DQ11	R14	DVDD_MDSYS	AD20	RFIC0_BSI_EN
E16	EMI_TN	R15	DVSS	AD21	RFIC0_BSI_CK
E17	EMI1_CK_C	R16	DVDD_TOP	AD22	BPI_ANT0
E18	EMI1_CS0	R17	DVDD_TOP	AD23	INT_SIM1
E19	EMI1_CA5	R18	DVDD_TOP	AD24	BPI_BUS9
E21	EMI1_DQ0	R19	DVSS	AD25	DVSS
E22	DVSS	R20	DVSS	AD26	AVDD18_CPU
E23	DVSS	R21	DVDD_MFGSYS	AD27	SIM2_SRST
E26	DVSS	R22	DVSS	AE2	KPROW1
E27	NC	R25	DSI0_CKP	AE3	SPI_MI
E29	VQPS	R26	DSI0_D2N	AE4	SPI_CLK
F3	GPS_RXIP	R27	DSI0_D1N	AE5	SCL0
F4	WB_CTRL3	T1	CSI0A_L1P	AE6	BPI_BUS0
F5	WB_CTRL4	T2	CSI0A_L1N	AE7	BPI_BUS2
F10	EMI0_CS0	T3	DVSS	AE8	DVDD18_IORB
F11	EMI0_DQ13	T4	CSI0B_L0N	AE9	MISC_BSI_CK_3
F12	DVSS	T5	CSI0A_L0P	AE10	MISC_BSI_CK_2
F13	DVSS	T7	DVDD_TOP	AE11	AVDD12_MD
F14	EMI1_DQ15	T11	DVDD_MDSYS	AE12	DET_IN0
F15	DVSS	T12	DVDD_TOP_SRAM	AE13	DET_QN0
F16	DVSS	T13	DVSS	AE15	PRX_BB_Q1
F17	EMI1_CA0	T14	DVDD_MDSYS	AE16	DRX_BB_Q1
F18	EMI1_CKE0	T15	DVSS	AE17	DRX_BB_I0
F19	EMI1_DQ2	T16	DVDD_TOP	AE18	DRX_BB_Q0

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F21	DVSS	T17	DVSS	AE19	DVSS
F22	DVSS	T18	DVDD_TOP	AE21	DVSS
F27	DVSS	T19	DVDD_MFG_SRAM	AE22	BPI_OLAT1
F28	AVDD12_USB	T20	DVDD_MFGSYS	AE23	BPI_BUS10
F29	AVDD33_USB	T21	DVDD_MFGSYS	AE25	SDA3
G1	GPS_RXQP	T22	DVSS	AE26	BPI_BUS8
G2	GPS_RXQN	T26	DSI0_D2P	AE27	SIM2_SCLK
G3	GPS_RXIN	T27	DSI0_D1P	AE28	DVDD28_SIM1
G4	DVSS	T28	DVSS	AE29	DVDD28_SIM2
G6	DVSS	T29	AVDD12_DSI	AF1	EINT8
G9	AVDD18_DDR	U1	AVDD12_CSI	AF2	PWM_A
G14	AVDD18_DDR	U2	SDA2	AF3	BPI_PA_VM1
G20	AVDD18_DDR	U3	SCL2	AF4	BPI_PA_VM0
G24	USB_DP	U4	EINT10	AF5	BPI_OLAT0
G25	CHD_DM	U5	DVSS	AF6	BPI_BUS6
G26	CHD_DP	U8	DVSS	AF7	BPI_BUS7
G28	AVDD18_USB	U10	DVDD_VDD_MODEM	AF8	CDM3P5A
H2	DVSS	U13	DVSS	AF9	MISC_BSI_CK_1
H3	WB_CTRL1	U14	DVDD_VDD_MODEM	AF10	MISC_BSI_DO_1
H4	WB_CTRL2	U15	DVDD_VDD_MODEM	AF11	MISC_BSI_CK_0
H5	DVSS	U18	DVSS	AF12	DVSS
H6	XIN_WBG	U19	DVSS	AF13	TX_BB_IP0
H9	AVDD2_EMI	U22	DVSS	AF14	TX_BB_IN0
H10	AVDDQ_EMI	U23	DVDD_TOP	AF15	DVSS
H12	AVDDQ_EMI	U25	DPI_D6	AF16	PRX_BB_I0
H13	AVDD2_EMI	U26	DPI_D5	AF17	PRX_BB_Q0
H14	AVDDQ_EMI	U27	DPI_D1	AF19	AVDD18_MD
H16	AVDDQ_EMI	U28	DPI_D3	AF20	AVDD18_AP
H17	AVDD2_EMI	U29	AVDD04_DSI	AF21	AUXIN2
H18	AVDD2_EMI	V2	SDA4	AF22	AUXIN3
H19	AVDDQ_EMI	V3	CAM_RST1	AF23	AUXIN0
H23	DVSS	V4	CAM_PDN0	AF25	SCL3
H24	USB_DM	V5	DVSS	AF26	DISP_PWM
H25	DVSS	V6	DVSS	AF27	DSI_TE
H26	DVSS	V8	DVSS	AF28	DRVBUS
H27	RTC32K_CK	V10	DVDD_VDD_MODEM	AF29	DVDD28_MSDC1
H28	TESTMODE	V12	DVDD_TOP_SRAM	AG1	NC
H29	DVDD18_IOLT	V13	DVSS	AG2	SCL1
J1	AVDD18_WBG	V16	DVDD_MCUSYS_SRA M	AG3	SDA1
J2	AVDD12_WBG	V17	DVSS	AG5	BPI_ANT1
J3	WB_SCLK	V18	DVDD_MCUSYS	AG6	BPI_BUS5
J4	WB_RSTB	V23	DVSS	AG8	CDM5P5A
J5	WB_CTRL0	V25	DPI_CK	AG9	DVDD18_IOBR
J6	DVSS	V26	DPI_D4	AG11	MISC_BSI_DO_0

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
J9	DVSS	V27	DPI_D8	AG12	AVDD18_MD
J16	DVDD_TOP	V28	DPI_D2	AG14	TX_BB_QP0
J21	DVDD_TOP	W1	DVDD18_IORB	AG15	TX_BB_QN0
J23	DVDD_TOP	W2	SCL4	AG17	DVSS
J25	AUD_CLK_MISO	W3	SRCLKENAI	AG19	REFP
J26	WATCHDOG	W4	CAM_RST0	AG21	AUXIN1
J27	SYSRSTB	W5	CAM_PDN1	AG23	AUXIN4
J28	AUD_DAT_MOSI0	W8	DVSS	AG25	DVDD18_IOBL
K2	DVDD18_IORT	W10	DVDD_VDD_MODEM	AG26	LCM_RST
K3	ANT_SEL2	W12	TN_PLLGP	AG28	IDDIG
K4	WB_SDATA	W13	TP_PLLGP	AG29	NC
K5	WB_SEN	W14	DVDD_VDD_MODEM		
K9	DVSS	W16	DVDD_MCUSYS		

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-3. Detailed pin description (using LPDDR4)

Pin name	Pin no.	Type	Description	Power domain
SYSTEM				
SYSRSTB	J27	DI	System reset input	DVDD18
WATCHDOG	J26	DIO	Watchdog reset output	DVDD18
TESTMODE	H28	DI	Test mode	DVDD18
RTC32K_CK	H27	DIO	RTC 32K input	DVDD18
SRCLKENA0	N24	DIO	Output signal; control 26Hz/Buck/LDO normal mode or sleep mode. (High: normal mode, Low: sleep mode or low power mode)	DVDD18
SRCLKENA1	M25	DIO	Output signal; control VRF18. (High: VRF18 on, Low: VRF18 off)	DVDD18
SRCLKENAI	W3	DIO	Input signal; NFC 26MHz request signal. (High: NFC chip requests system to provide 26MHz to NFC chip)	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
EINT0	AC5	DIO	External interrupt input	DVDD18
EINT1	AB3	DIO	External interrupt input	DVDD18
EINT2	AC3	DIO	External interrupt input	DVDD18
EINT3	AB2	DIO	External interrupt input	DVDD18
EINT4	AA2	DIO	External interrupt input	DVDD18
EINT5	AB4	DIO	External interrupt input	DVDD18
EINT6	AC4	DIO	External interrupt input	DVDD18
EINT7	AB5	DIO	External interrupt input	DVDD18
EINT8	AF1	DIO	External interrupt input	DVDD18
EINT9	AA1	DIO	External interrupt input	DVDD18
EINT10	U4	DIO	External interrupt input	DVDD18
EINT11	M26	DIO	External interrupt input	DVDD18
EINT12	M24	DIO	External interrupt input	DVDD18
PMIC				
PWRAP_SPI0_MO	M28	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_MI	M27	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CSN	L27	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CK	M29	DIO	PMIC SPI control interface	DVDD18
AUD_CLK_MOSI	K28	DIO	PMIC audio input interface	DVDD18
AUD_CLK_MISO	J25	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MISO	K25	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MOSI	K27	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO0	L26	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO1	L25	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI0	J28	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI1	K29	DIO	PMIC audio input interface	DVDD18
SIM				
SIM1_SCLK	AB25	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	AC26	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	AC25	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	AE27	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	AC27	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	AD27	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	AD23	DIO	SIM1 interrupt	DVDD18
INT_SIM2	AC23	DIO	SIM2 interrupt	DVDD18
LCD				
DSI_TE	AF27	DIO	Parallel display interface tearing effect	DVDD18
LCM_RST	AG26	DIO	Parallel display interface reset signal	DVDD18
DPI_HSYNC	W26	DIO	Parallel display interface HSYNC	DVDD18
DPI_VSYNC	W25	DIO	Parallel display interface VSYNC	DVDD18
DPI_CK	V25	DIO	Parallel display interface CLK	DVDD18
DPI_DE	W24	DIO	Parallel display interface DE	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
DPI_D11	Y27	DIO	Data pin 11 for DPI parallel LCD interface	DVDD18
DPI_D10	AA27	DIO	Data pin 10 for DPI parallel LCD interface	DVDD18
DPI_D9	AA28	DIO	Data pin 9 for DPI parallel LCD interface	DVDD18
DPI_D8	V27	DIO	Data pin 8 for DPI parallel LCD interface	DVDD18
DPI_D7	W28	DIO	Data pin 7 for DPI parallel LCD interface	DVDD18
DPI_D6	U25	DIO	Data pin 6 for DPI parallel LCD interface	DVDD18
DPI_D5	U26	DIO	Data pin 5 for DPI parallel LCD interface	DVDD18
DPI_D4	V26	DIO	Data pin 4 for DPI parallel LCD interface	DVDD18
DPI_D3	U28	DIO	Data pin 3 for DPI parallel LCD interface	DVDD18
DPI_D2	V28	DIO	Data pin 2 for DPI parallel LCD interface	DVDD18
DPI_D1	U27	DIO	Data pin 1 for DPI parallel LCD interface	DVDD18
DPI_D0	W27	DIO	Data pin 0 for DPI parallel LCD interface	DVDD18
PWM				
PWM_A	AF2	DIO	PWM_A	DVDD18
DISP_PWM	AF26	DIO	Display PWM	DVDD18
Keypad Interface				
KPCOL0	AC2	DIO	Keypad column 0	DVDD18
KPCOL1	AC1	DIO	Keypad column 1	DVDD18
KPROW0	AD2	DIO	Keypad row 0	DVDD18
KPROW1	AE2	DIO	Keypad row 1	DVDD18
SPI				
SPI_CSB	AD3	DIO	SPI chip select	DVDD18
SPI_MI	AE3	DIO	SPI data in	DVDD18
SPI_MO	AD4	DIO	SPI data out	DVDD18
SPI_CLK	AE4	DIO	SPI clock	DVDD18
UR				
UTXD0	AA3	DIO	UR interdace	DVDD18
URXD0	Y3	DIO	SPI data in	DVDD18
BPI				
BPI_BUS0	AE6	DIO	BPI_BUS0	DVDD18
BPI_BUS1	AD6	DIO	BPI_BUS1	DVDD18
BPI_BUS2	AE7	DIO	BPI_BUS2	DVDD18
BPI_BUS3	AD7	DIO	BPI_BUS3	DVDD18
BPI_BUS4	AC7	DIO	BPI_BUS4	DVDD18
BPI_BUS5	AG6	DIO	BPI_BUS5	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
BPI_BUS6	AF6	DIO	BPI_BUS6	DVDD18
BPI_BUS7	AF7	DIO	BPI_BUS7	DVDD18
BPI_BUS8	AE26	DIO	BPI_BUS8	DVDD18
BPI_BUS9	AD24	DIO	BPI_BUS9	DVDD18
BPI_BUS10	AE23	DIO	BPI_BUS10	DVDD18
BPI_ANT0	AD22	DIO	BPI_ANT0	DVDD18
BPI_ANT1	AG5	DIO	BPI_ANT1	DVDD18
BPI_ANT2	AC24	DIO	BPI_ANT2	DVDD18
BPI_PA_VM0	AF4	DIO	PA_VM0	DVDD18
BPI_PA_VM1	AF3	DIO	PA_VM1	DVDD18
BPI_OLAT0	AF5	DIO	BPI control	DVDD18
BPI_OLAT1	AE22	DIO	BPI control	DVDD18
ANT_SEL0	L1	DIO	BPI control	DVDD18
ANT_SEL1	L2	DIO	BPI control	DVDD18
ANT_SEL2	K3	DIO	BPI control	DVDD18
BSI				
RFIC0_BSI_CK	AD21	DIO	RFIC0 BSI CLK	DVDD18
RFIC0_BSI_D0	AC21	DIO	RFIC0 BSI DATA0	DVDD18
RFIC0_BSI_D1	AC19	DIO	RFIC0 BSI DATA1	DVDD18
RFIC0_BSI_D2	AD19	DIO	RFIC0 BSI DATA2	DVDD18
RFIC0_BSI_EN	AD20	DIO	RFIC0 BSI CS	DVDD18
MISC_BSI_DO_0	AG11	DIO	MISC_BSI_DO_0	DVDD18
MISC_BSI_CK_0	AF11	DIO	MISC_BSI_CK_0	DVDD18
MISC_BSI_DO_1	AF10	DIO	MISC_BSI_DO_1	DVDD18
MISC_BSI_CK_1	AF9	DIO	MISC_BSI_CK_1	DVDD18
MISC_BSI_DO_2	AD8	DIO	MISC_BSI_DO_2	DVDD18
MISC_BSI_CK_2	AE10	DIO	MISC_BSI_CK_2	DVDD18
MISC_BSI_DO_3	AD9	DIO	MISC_BSI_DO_3	DVDD18
MISC_BSI_CK_3	AE9	DIO	MISC_BSI_CK_3	DVDD18
MSDC0				
MSDC0_CLK	D25	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	B24	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	A22	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	B23	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	A23	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	C24	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	B25	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	C26	DIO	MSDC0 data5 pin	DVDD18_MSDC0
MSDC0_DAT6	D24	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	A25	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	B26	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	C25	DIO	MSDC0 Reset pin	DVDD18_MSDC0

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Pin name	Pin no.	Type	Description	Power domain
MSDC1				
MSDC1_CLK	AA26	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	Y24	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	AC28	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	AA25	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	AB28	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	Y25	DIO	MSDC1 data3 pin	DVDD28_MSDC1
EFUSE				
VQPS	E29	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI				
EMI0_DQ0	E6	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ1	C6	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ2	D6	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ3	D7	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ4	A6	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ5	B7	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ6	B6	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ7	A5	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ8	C12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ9	E12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ10	A12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ11	B12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ12	C13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ13	F11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ14	B11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ15	D12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS0_C	D5	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS0_T	C5	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS1_C	D13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS1_T	E13	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA0	E10	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA1	A10	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA2	A8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA3	C8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA4	C9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA5	E7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS0	F10	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS1	C10	DIO	DRAM interface	AVDDQ_EMI
EMI0_DMI0	B8	DIO	DRAM interface	AVDDQ_EMI
EMI0_DMI1	B10	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE0	D9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE1	E9	DIO	DRAM interface	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
EMI0_CK_C	E11	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_T	D11	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ0	E21	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ1	D21	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ2	F19	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ3	D20	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ4	C20	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ5	B20	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ6	A20	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ7	C21	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ8	A14	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ9	C14	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ10	B14	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ11	E15	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ12	C15	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ13	A16	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ14	B15	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ15	F14	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS0_C	C22	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS0_T	D22	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS1_C	E14	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS1_T	D14	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA0	F17	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA1	C16	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA2	B18	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA3	A18	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA4	C18	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA5	E19	DIO	DRAM interface	AVDDQ_EMI
EMI1_CS0	E18	DIO	DRAM interface	AVDDQ_EMI
EMI1_CS1	C17	DIO	DRAM interface	AVDDQ_EMI
EMI1_DMI0	B19	DIO	DRAM interface	AVDDQ_EMI
EMI1_DMI1	B16	DIO	DRAM interface	AVDDQ_EMI
EMI1_CKE0	F18	DIO	DRAM interface	AVDD2_EMI
EMI1_CKE1	D19	DIO	DRAM interface	AVDD2_EMI
EMI1_CK_C	E17	DIO	DRAM interface	AVDDQ_EMI
EMI1_CK_T	D17	DIO	DRAM interface	AVDDQ_EMI
EMI_EXTR	B5	DIO	DRAM interface	AVDD2_EMI
EMI_RESET_N	D23	DIO	DRAM interface	AVDD2_EMI
EMI_TP	D16	DIO	DRAM interface	AVDD2_EMI
EMI_TN	E16	DIO	DRAM interface	AVDD18_DDR
AVDD18_DDR	G9	P	DRAM power	AVDD18_DDR

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Pin name	Pin no.	Type	Description	Power domain
AVDD18_DDR	G14	P	DRAM power	AVDD18_DDR
AVDD18_DDR	G20	P	DRAM power	AVDD18_DDR
AVDD2_EMI	H9	P	DRAM power	AVDD2_EMI
AVDD2_EMI	H13	P	DRAM power	AVDD2_EMI
AVDD2_EMI	H17	P	DRAM power	AVDD2_EMI
AVDD2_EMI	H18	P	DRAM power	AVDD2_EMI
AVDDQ_EMI	H10	P	DRAM power	AVDDQ_EMI
AVDDQ_EMI	H12	P	DRAM power	AVDDQ_EMI
AVDDQ_EMI	H14	P	DRAM power	AVDDQ_EMI
AVDDQ_EMI	H16	P	DRAM power	AVDDQ_EMI
AVDDQ_EMI	H19	P	DRAM power	AVDDQ_EMI
CAM				
CAM_CLK0	Y4	DIO	Master clock to 1st sensor	DVDD18
CAM_CLK1	Y5	DIO	Master clock to 2nd sensor	DVDD18
CAM_RST0	W4	DIO	Reset control to 1st sensor	DVDD18
CAM_PDN0	V4	DIO	Power down to 1st sensor	DVDD18
CAM_RST1	V3	DIO	Reset control to 2nd sensor	DVDD18
CAM_PDN1	W5	DIO	Power down to 2nd sensor	DVDD18
I2C				
SCL0	AE5	DIO	I2C0 clock	DVDD18
SCL1	AG2	DIO	I2C1 clock	DVDD18
SCL2	U3	DIO	I2C2 clock	DVDD18
SCL3	AF25	DIO	I2C3 clock	DVDD18
SCL4	W2	DIO	I2C4 clock	DVDD18
SCL_APPM	AB24	DIO	I2C clock	DVDD18
SDA0	AD5	DIO	I2C0 data	DVDD18
SDA1	AG3	DIO	I2C1 data	DVDD18
SDA2	U2	DIO	I2C2 data	DVDD18
SDA3	AE25	DIO	I2C3 data	DVDD18
SDA4	V2	DIO	I2C4 data	DVDD18
SDA_APPM	AB27	DIO	I2C data	DVDD18
CONN				
WB_CTRL0	J5	DIO	WB control for CONN_RF	DVDD18
WB_CTRL1	H3	DIO	WB control for CONN_RF	DVDD18
WB_CTRL2	H4	DIO	WB control for CONN_RF	DVDD18
WB_CTRL3	F4	DIO	WB control for CONN_RF	DVDD18
WB_CTRL4	F5	DIO	WB control for CONN_RF	DVDD18
WB_CTRL5	E4	DIO	WB control for CONN_RF	DVDD18
WB_RSTB	J4	DIO	Reset for CONN_RF	DVDD18
WB_SEN	K5	DIO	SPI for CONN_RF	DVDD18
WB_SCLK	J3	DIO	SPI for CONN_RF	DVDD18
WB_SDATA	K4	DIO	SPI for CONN_RF	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
F2W_CLK	L4	DIO	AUD_IN from CONN_RF	DVDD18
F2W_DATA	L3	DIO	AUD_IN from CONN_RF	DVDD18
ABB				
REFP	AG19	AIO	ABB interface	AVDD18_MD
AUXIN0	AF23	AIO	ABB interface	AVDD18_MD
AUXIN1	AG21	AIO	ABB interface	AVDD18_MD
AUXIN2	AF21	AIO	ABB interface	AVDD18_MD
AUXIN3	AF22	AIO	ABB interface	AVDD18_MD
AUXIN4	AG23	AIO	ABB interface	AVDD18_MD
MAIN_X26M_IN	AC14	AIO	ABB interface	AVDD18_MD
PRX_BB_Q1	AE15	AIO	ABB interface	AVDD18_MD
PRX_BB_I1	AD15	AIO	ABB interface	AVDD18_MD
DRX_BB_Q1	AE16	AIO	ABB interface	AVDD18_MD
DRX_BB_I1	AD16	AIO	ABB interface	AVDD18_MD
DET_IN0	AE12	AIO	ABB interface	AVDD18_MD
DET_IP0	AD12	AIO	ABB interface	AVDD18_MD
DET_QP0	AD13	AIO	ABB interface	AVDD18_MD
DET_QN0	AE13	AIO	ABB interface	AVDD18_MD
TX_BB_QP0	AG14	AIO	ABB interface	AVDD18_MD
TX_BB_QN0	AG15	AIO	ABB interface	AVDD18_MD
TX_BB_IN0	AF14	AIO	ABB interface	AVDD18_MD
TX_BB_IP0	AF13	AIO	ABB interface	AVDD18_MD
PRX_BB_Q0	AF17	AIO	ABB interface	AVDD18_MD
PRX_BB_I0	AF16	AIO	ABB interface	AVDD18_MD
DRX_BB_Q0	AE18	AIO	ABB interface	AVDD18_MD
DRX_BB_I0	AE17	AIO	ABB interface	AVDD18_MD
APC	AD11	AIO	ABB interface	AVDD18_MD
MIPI				
DSI0_D3N	P28	AIO	DSI interface	AVDD12_DSI
DSI0_D3P	P29	AIO	DSI interface	AVDD12_DSI
DSI0_D1N	R27	AIO	DSI interface	AVDD12_DSI
DSI0_D1P	T27	AIO	DSI interface	AVDD12_DSI
DSI0_CKN	P25	AIO	DSI interface	AVDD12_DSI
DSI0_CKP	R25	AIO	DSI interface	AVDD12_DSI
DSI0_D0N	P26	AIO	DSI interface	AVDD12_DSI
DSI0_D0P	P27	AIO	DSI interface	AVDD12_DSI
DSI0_D2N	R26	AIO	DSI interface	AVDD12_DSI
DSI0_D2P	T26	AIO	DSI interface	AVDD12_DSI
CSI0A_L0P	T5	AO	CSI interface	AVDD12_CSI
CSI0A_L0N	R5	AIO	CSI interface	AVDD12_CSI
CSI0A_L1P	T1	AIO	CSI interface	AVDD12_CSI
CSI0A_L1N	T2	AIO	CSI interface	AVDD12_CSI

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Pin name	Pin no.	Type	Description	Power domain
CSI0A_L2P	R2	AIO	CSI interface	AVDD12_CSI
CSI0A_L2N	R3	AIO	CSI interface	AVDD12_CSI
CSI0B_L0P	R4	AIO	CSI interface	AVDD12_CSI
CSI0B_L0N	T4	AIO	CSI interface	AVDD12_CSI
CSI0B_L1P	P3	AIO	CSI interface	AVDD12_CSI
CSI0B_L1N	P4	AIO	CSI interface	AVDD12_CSI
CSI1A_L0P	N5	AIO	CSI interface	AVDD12_CSI
CSI1A_L0N	M5	AIO	CSI interface	AVDD12_CSI
CSI1A_L1P	P2	AIO	CSI interface	AVDD12_CSI
CSI1A_L1N	P1	AIO	CSI interface	AVDD12_CSI
CSI1A_L2P	N4	AIO	CSI interface	AVDD12_CSI
CSI1A_L2N	N3	AIO	CSI interface	AVDD12_CSI
CSI1B_L0P	M3	AIO	CSI interface	AVDD12_CSI
CSI1B_L0N	M4	AIO	CSI interface	AVDD12_CSI
CSI1B_L1P	M1	AIO	CSI interface	AVDD12_CSI
CSI1B_L1N	M2	AIO	CSI interface	AVDD12_CSI
USB				
USB_DM	H24	AIO	USB D+ differential data line	AVDD33_USB
USB_DP	G24	AIO	USB D- differential data line	AVDD33_USB
CHD_DM	G25	AIO	BC1.1 charger DP	AVDD33_USB
CHD_DP	G26	AIO	BC1.1 charger DM	AVDD33_USB
WBG				
WB_RXQN	B1	AIO	RX_QN for WIFI/BT Rx	AVDD18_WBG
WB_RXQP	B2	AIO	RX_QP for WIFI/BT Rx	AVDD18_WBG
WB_RXIP	A3	AIO	RX_IN for WIFI/BT Rx	AVDD18_WBG
WB_RXIN	B3	AIO	RX_IP for WIFI/BT Rx	AVDD18_WBG
WB_TXQP	E2	AIO	TX_QP for WIFI/BT Tx	AVDD18_WBG
WB_TXQN	E1	AIO	TX_QN for WIFI/BT Tx	AVDD18_WBG
WB_TXIN	D2	AIO	TX_IN for WIFI/BT Tx	AVDD18_WBG
WB_TXIP	D3	AIO	TX_IP for WIFI/BT Tx	AVDD18_WBG
GPS_RXQN	G2	AIO	RX_QN for GPS Rx	AVDD18_WBG
GPS_RXQP	G1	AIO	RX_QP for GPS Rx	AVDD18_WBG
GPS_RXIP	F3	AIO	RX_IN for GPS Rx	AVDD18_WBG
GPS_RXIN	G3	AIO	RX_IP for GPS Rx	AVDD18_WBG
XIN_WBG	H6	AIO	26MHz clock input for WBG	AVDD18_WBG
MISC				
DRVBUS	AF28	DIO	This signal enables to drive 5V on Vbus. 0: Not drive Vbus 1: Drive 5V on Vbus	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
IDDIG	AG28	DIO	Indicates whether the connected plug is a mini-A or mini-B 0: Connected plug is a mini-A (ID is connected to GND). 1: Connected plug is a mini-B (ID is floating).	DVDD18
TN_PLLGP	W12	AIO	Reserved	-
TP_PLLGP	W13	AIO	Reserved	-
Analog Power				
AVDD04_DSI	U29	P	Analog power for DSI	-
AVDD12_AP	A27	P	Analog power for AP	-
AVDD12_MD	AE11	P	Analog power for modem	-
AVDD12_PLLGP	AA13	P	Analog power for PLL	-
AVDD12_USB	F28	P	Analog power for USB	-
AVDD12_DSI	T29	P	Analog power for DSI	-
AVDD12_CSI	U1	P	Analog power for CSI	-
AVDD12_WBG	J2	P	Analog power for WBG	-
AVDD18_AP	AF20	P	Analog power input 1.8V	-
AVDD18_CPU	AD26	P	Analog power input 1.8V for CPU	-
AVDD18_MD	AF19	P	Analog power input 1.8V for modem	-
AVDD18_PLLGP	Y13	P	Analog power input 1.8V for PLL	-
AVDD18_USB	G28	P	Analog power 1.8V for USB	-
AVDD18_WBG	J1	P	Analog power 1.8V for WBG (Wi-Fi, BT, GPS)	-
AVDD18_USB	G28	P	Analog power 1.8V for USB	-
AVDD33_USB	F29	P	Analog power 3.3V for USB	-
Digital Power				
DVDD_MCUSYS	V18, ...	P	Digital power input for DVFS	-
DVDD_TOP	J16, ...	P	Digital power input for Vcore	-
DVDD_MFGSYS	K21, ...	P	Digital power input for GPU	-
DVDD_VDD_MODEM	R9, ...	P	Digital power input for LTE	-
DVDD_MDSYS	N11, ...	P	Digital power input for LTE	-
DVDD_TOP_SRAM	K18, ...	P	Digital power input for SRAM	-
DVDD_MCUSYS_SRAM	V16, ...	P	Digital power input for DVFS SRAM	-
DVDD_MFG_SRAM	T19, ...	P	Digital power input for GPU SRAM	-
DVDD18_IOLT	H29	P	Digital power input for IO (region 1)	-
DVDD18_IOLM	W29	P	Digital power input for IO (region 2)	-
DVDD18_IOBL	AG25	P	Digital power input for IO (region 3)	-
DVDD18_IOBR	AG9	P	Digital power input for IO (region 4)	-
DVDD18_IORB	W1, ...	P	Digital power input for IO (region 5)	-
DVDD18_IORT	K2	P	Digital power input for IO (region 6)	-
DVDD18_MSDC0	A26	P	Digital power input for MSDC0	-
DVDD18_MSDC1	AA29	P	Digital power input for MSDC1	-
DVDD28_MSDC1	AF29	P	Digital power input for MSDC1	-

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Pin name	Pin no.	Type	Description	Power domain
DVDD18_SIM	AC29	P	Digital power input for SIM1/2	-
DVDD28_SIM1	AE28	P	Digital power input for SIM1	-
DVDD28_SIM2	AE29	P	Digital power input for SIM2	-
ESD				
CDM3P5A	AK1	G	Analog ground input for modem	-
CDM5P5A	AL1	G	Analog ground input for WBG	-
Digital Ground				
DVSS	B4, ...	G	Ground input	-
Misc				
NC	A1, ...	-	Not connected	-

Table 2-4. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or pin name	Description	Max.	Unit
AVDD18_DDR AVDD18_PLLGP	Analog power input 1.8V for PLL & DDR	1.89	V
AVDD12_PLLGP			V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.89	V
AVDD12_MD			V
AVDD28_DAC	Analog power input 2.8V for APC	2.94	V
AVDD12_CSI			
AVDD12_DSI			
AVDD04_DSI			
AVDD33_USB_P0	Analog power 3.3V for USB	3.22	V
AVDD18_USB	Analog power 1.8V for USB	1.89	V
AVDD12_USB			
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.89	V
AVDD12_WBG			
DVDD18_IOTL DVDD18_IOLT DVDD18_IOLM DVDD18_SIM DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT DVDD18_MC1	Digital power input for 1.8V IO	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1. 95	V
DVDD28_MSDC1	Digital power input for MSDC1	3.3	V
DVDD28_SIM1	Digital power input for SIM1	3.3	V
DVDD28_SIM2	Digital power input for SIM2	3.3	V
DVDD2 DVDDQ	Digital power input for DRAM	1.155	V
DVDD_DVFS_SRAM	Digital power input for SRAM		V
DVDD_DVFS	Digital power input for DVFS	1.076	V
DVDD_MFG_SRAM	Digital power input for SRAM		V
DVDD_MFG	Digital power input for GPU	0.945	V
DVDD_MD1	Digital power input for MD1	0.735	V
DVDD_MODEM	Digital power input for MODEM	0.84	V
DVDD_TOP_SRAM	Digital power input for SRAM		V
DVDD_TOP	Digital power input for TOP	0.84	V

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Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_DDR AVDD18_PLLGP	Analog power input 1.8V for PLL & DDR	1.71	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AUXADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD12_MD					
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
AVDD12_CSI					
AVDD12_DSI					
AVDD04_DSI					
AVDD33_USB_P0	Analog power 3.3V for USB	2.92	3.07	3.22	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD12_USB					
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
AVDD12_WBG					
DVDD18_IOTL DVDD18_IOLT DVDD18_IOLM DVDD18_SIM DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.7	1.8	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7 2.7	1.8 3.0	1.9 3.3	V
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7 1.68	3 1.8	3.3 1.92	V
DVDD2 DVDDQ	Digital power input for EMI (LPDDR3/4)	1.045	1.1	1.155	V
DVDD_DVFS_SRAM					V
DVDD_DVFS	Digital power input for DVFS	0.57 0.665 0.76 0.855 0.973	0.6 0.7 0.8 0.9 1.025	0.63 0.735 0.84 0.945 1.076	V
DVDD_MFG_SRAM		0.57	0.6	0.63	V
DVDD_MFG	Digital power input for GPU	0.855	0.9	0.945	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
		0.76	0.8	0.84	
		0.665	0.7	0.735	
		0.617	0.65	0.682	
		0.57	0.6	0.63	
DVDD_MD1	Digital power input for MD1	0.665	0.7	0.735	V
DVDD_MODEM	Digital power input for MODEM	0.76	0.8	0.84	V
		0.665	0.7	0.735	
DVDD_TOP_SRAM					V
DVDD_TOP	Digital power input for TOP	0.76	0.8	0.84	V
		0.665	0.7	0.735	

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
FRTC	Input clock frequency		32		kHz
DCRTC	Input signal duty cycle	45	50	55	%

2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V

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Parameters	Descriptions	Min.	Typ.	Max.	Unit
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

2.2.4.3 I2C0, I2C1, I2C2 DC Electrical Characteristics

Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.3		2.0	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125*	V

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Parameters	Descriptions	Min.	Typ.	Max.	Unit
				DVDD28_MSDC1	

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V)

Parameters	Descriptions	Min	Typ	Max	Unit
VIH	Input logic low voltage	1.27		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

2.2.4.7 SIM DC Electrical Characteristics

Table 2-14. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR3

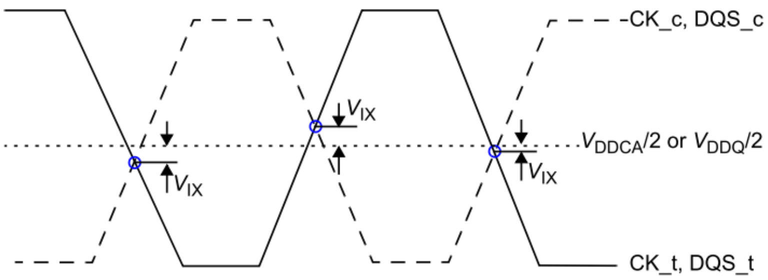

Figure 2-2. LPDDR3 VIX definition

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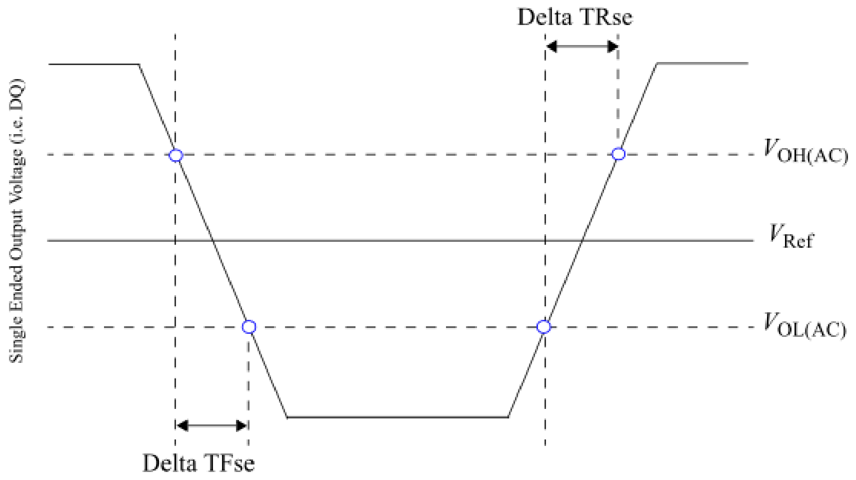

Figure 2-3. LPDDR3 single-ended output slew-rate definition

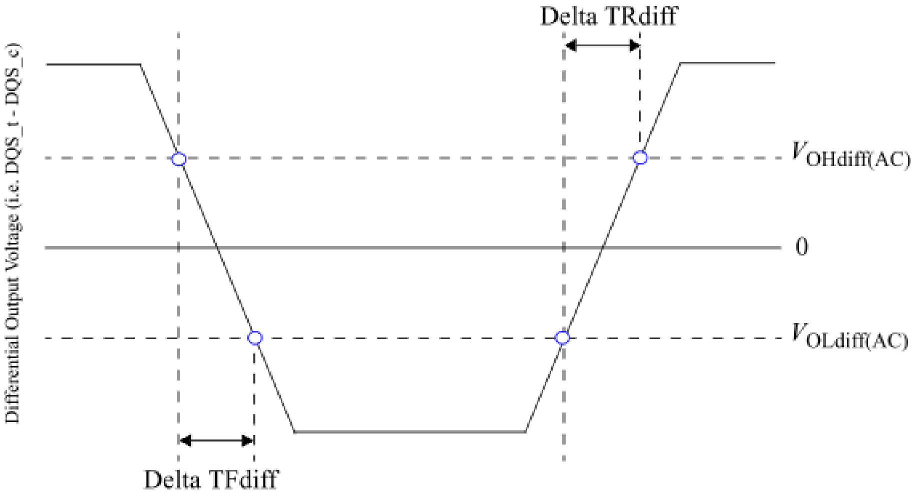

Figure 2-4. LPDDR3 differential output slew-rate definition

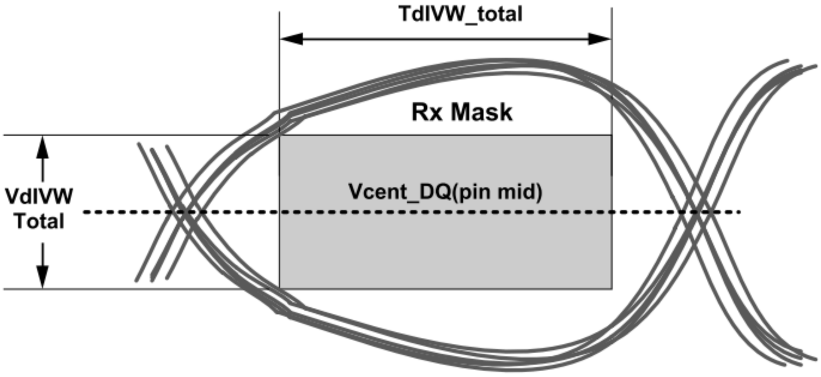

Figure 2-5. LPDDR3 RX mask

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Table 2-15. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
VIXCA	Differential input cross point voltage relative to VDDCA/2 for CK_t, CK_c	-120		120	mV
VIXDQ	Differential input cross point voltage relative to VDDQ/2 for DQS_t, DQS_c	-120		120	mV
SRQse	Single-ended output slew rate (RON = 40Ω +/- 30%)	1.5		4	V/ns
SRQdiff	Differential output slew rate (RON = 40Ω +/- 30%)	3		8	V/ns
VdIVW_total	Rx mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

2.2.5.2 External Memory Interface for LPDDR4/LPDDR4X

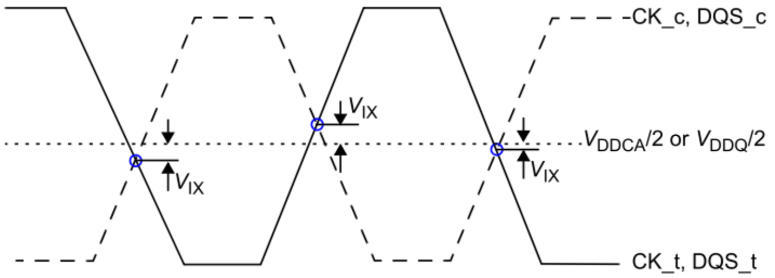

Figure 2-6. LPDDR4/LPDDR4X VIX definition

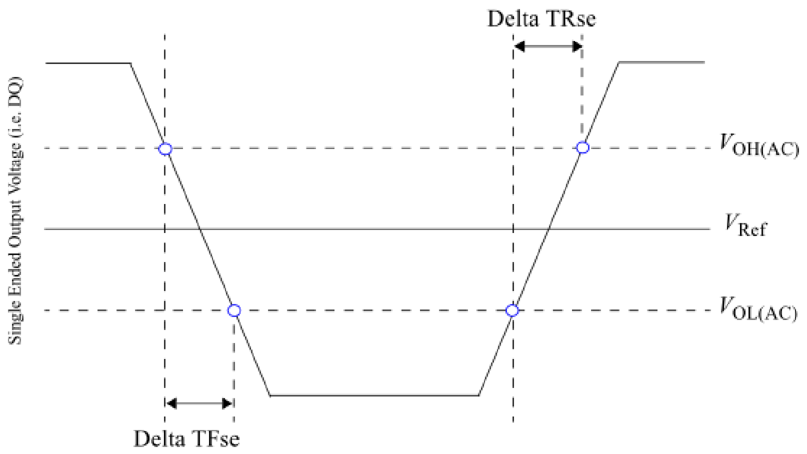

Figure 2-7. LPDDR4/LPDDR4X single-ended output slew-rate definition

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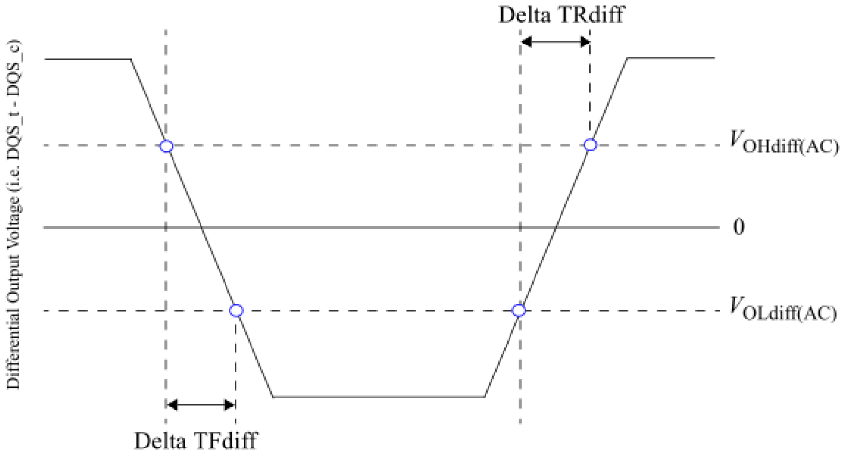

Figure 2-8. LPDDR4/LPDDR4X differential output slew-rate definition

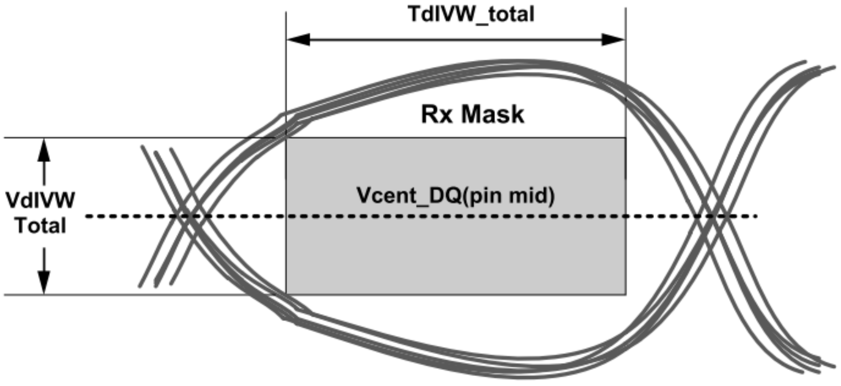

Figure 2-9. LPDDR4/LPDDR4X RX mask

Table 2-16. LPDDR4/LPDDR4X AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
Vix_DQS_ratio	DQS differential input crosspoint voltage ratio			20	%
Vix_CK_ratio	CK differential input crosspoint voltage ratio			25	%
SRQse (LPDDR4)	Single-ended output slew rate	3.5		9	V/ns
SRQse (LPDDR4X)	Single-ended output slew rate	3		9	V/ns
SRQdiff (LPDDR4)	Differential output slew rate	7		18	V/ns
SRQdiff (LPDDR4X)	Differential output slew rate	6		18	V/ns
VdIVW_total	Rx Mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

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2.2.5.3 SPI AC Timing Characteristics

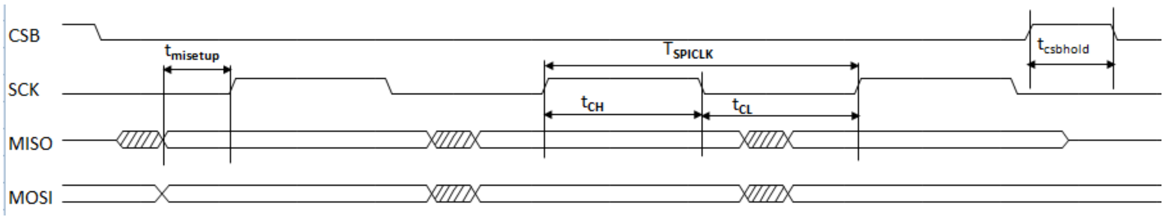

Figure 2-10. SPI timing diagram

Table 2-17. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	18.2	-	-	ns
SPI clock low time	t_{CL}	9.1	-	-	ns
SPI clock high time	t_{CH}	9.1	-	-	ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

2.2.5.4 I2S AC Timing Characteristics

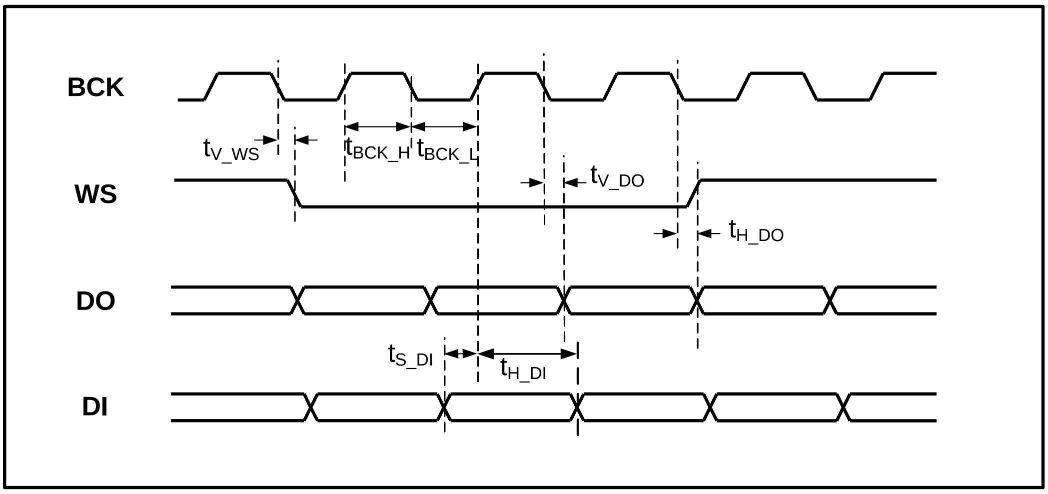

Figure 2-11. I2S master mode timing diagram

Table 2-18. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
fs	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz

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Parameter	Description	Min.	Typ.	Max.	Unit
f_{BCK}	Serial clock frequency	32 * f_S	-	64 * f_S	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

2.2.5.5 I2C AC Timing Characteristics

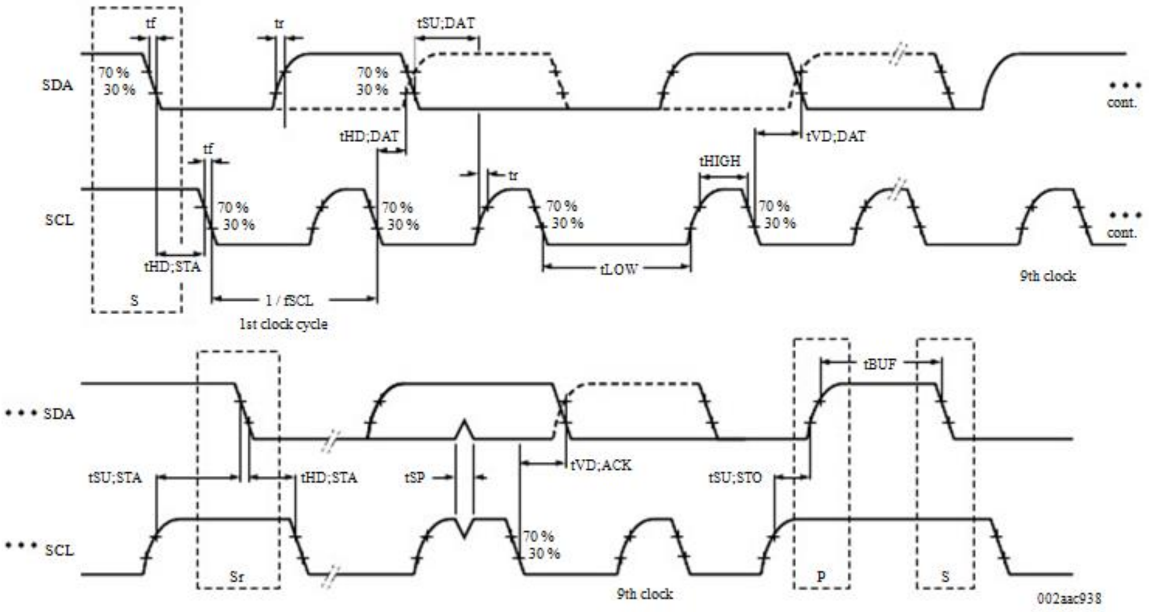

Figure 2-12. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-19. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration

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Symbol	Standard mode	Fast mode	Unit	Note
				register.

2.2.5.6 MSDC AC Timing Characteristics

2.2.5.6.1 Default Speed Timing

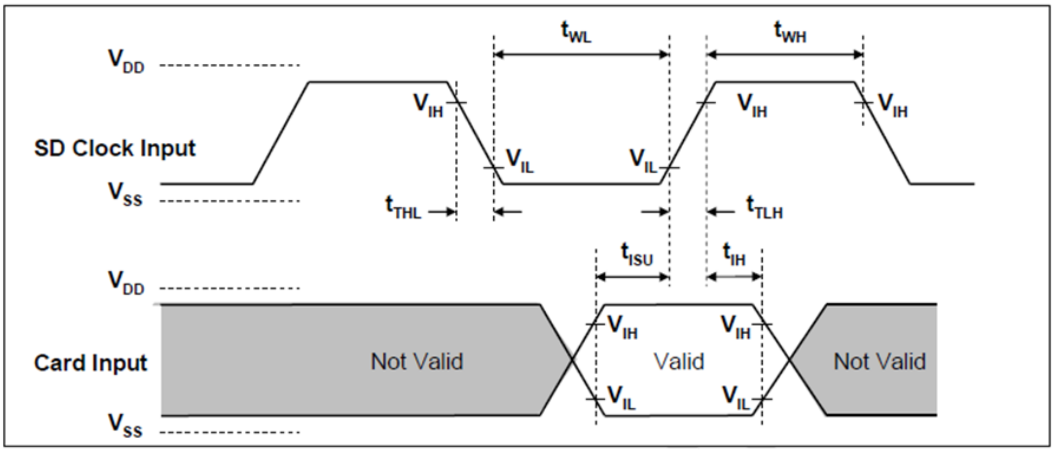

Figure 2-13. MSDC input timing diagram of default speed

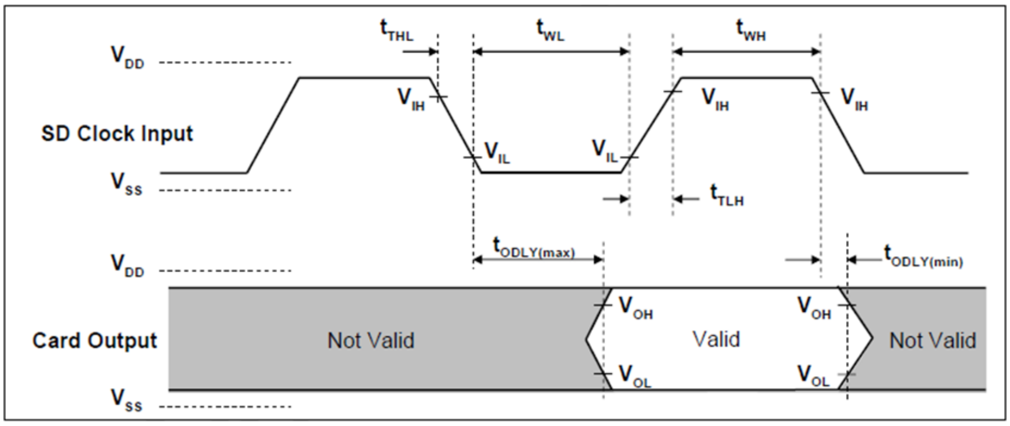

Figure 2-14. MSDC output timing diagram of default speed

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Table 2-20. MSDC AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD}≦10pF (1 card)
Clock frequency identification mode	f_{OD}	0[(1)] / 100	400	kHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD}≦10pF (1 card)
Input hold time	T_{IH}	5		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L≦40pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L≦40pF (1 card)

2.2.5.6.2 High Speed Timing

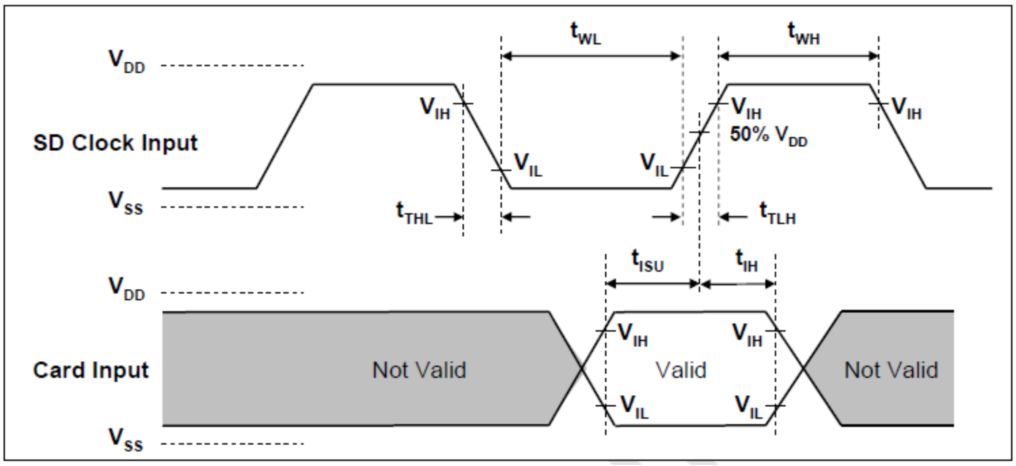

Figure 2-15. MSDC input timing diagram of high speed

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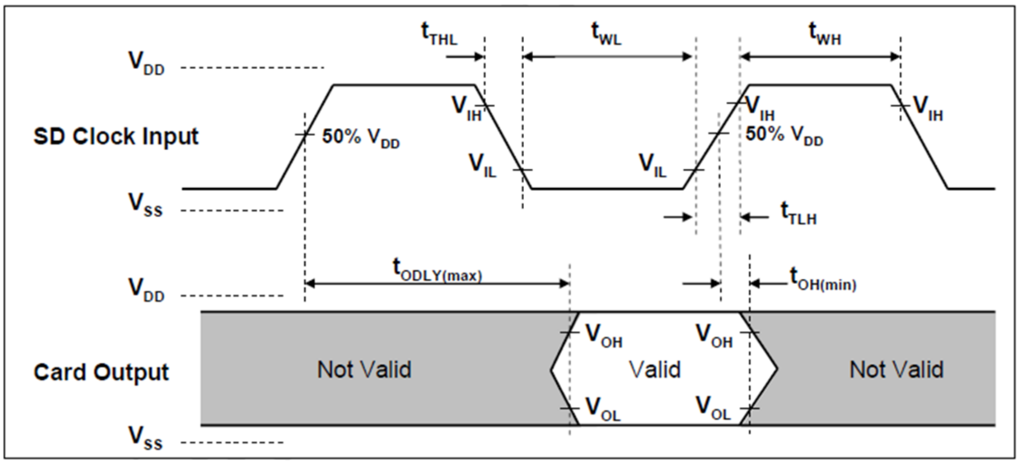

Figure 2-16. MSDC output timing diagram of high speed

Table 2-21. MSDC AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	$C_{CARD}\leqq$10pF (1 card)
Clock low time	t_{WL}	7		ns	$C_{CARD}\leqq$10pF (1 card)
Clock high time	t_{WH}	7		ns	$C_{CARD}\leqq$10pF (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{CARD}\leqq$10pF (1 card)
Clock fall time	t_{THL}		3	ns	$C_{CARD}\leqq$10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	$C_{CARD}\leqq$10pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{CARD}\leqq$10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	$C_L\leqq$40pF (1 card)
Output hold time	t_{OH}	2.5		ns	$C_L\geqq$15pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.6.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

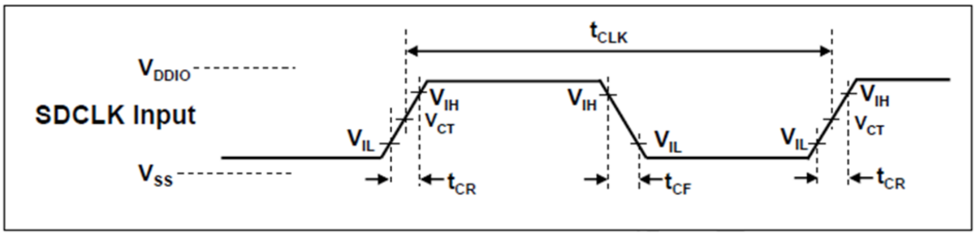

Figure 2-17. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

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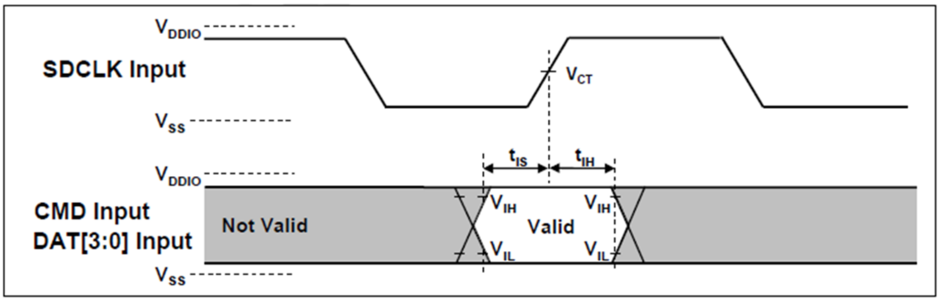

Figure 2-18. MSDC input timing diagram of SDR50/SDR104 mode

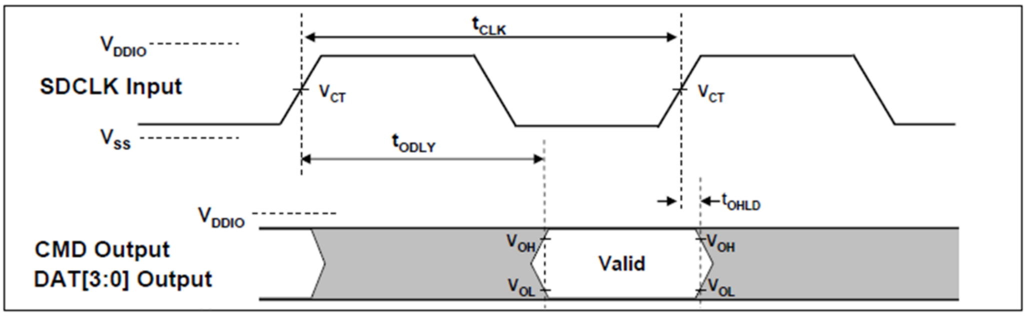

Figure 2-19. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50)

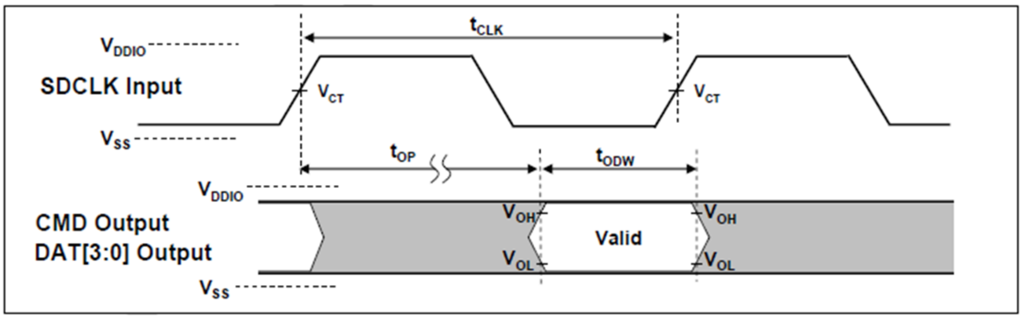

Figure 2-20. MSDC output timing diagram of variable window (SDR104)

Table 2-22. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (Max), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

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Symbol	Min.	Max.	Unit	Remark
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	t_{CLK}≧10.0ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	t_{CLK}≧20.0ns, C_L=40pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.6.4 DDR50 Speed Mode Timing

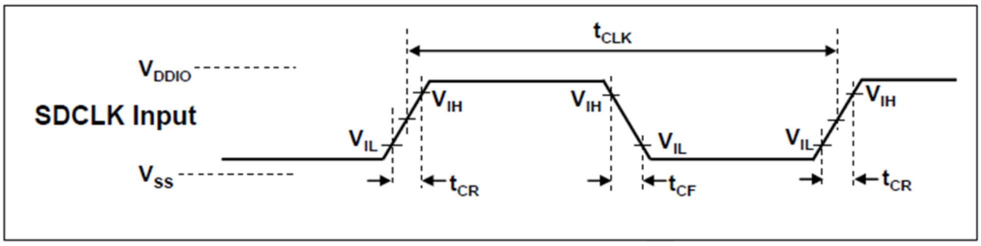

Figure 2-21. MSDC clock timing diagram of DDR50 speed mode

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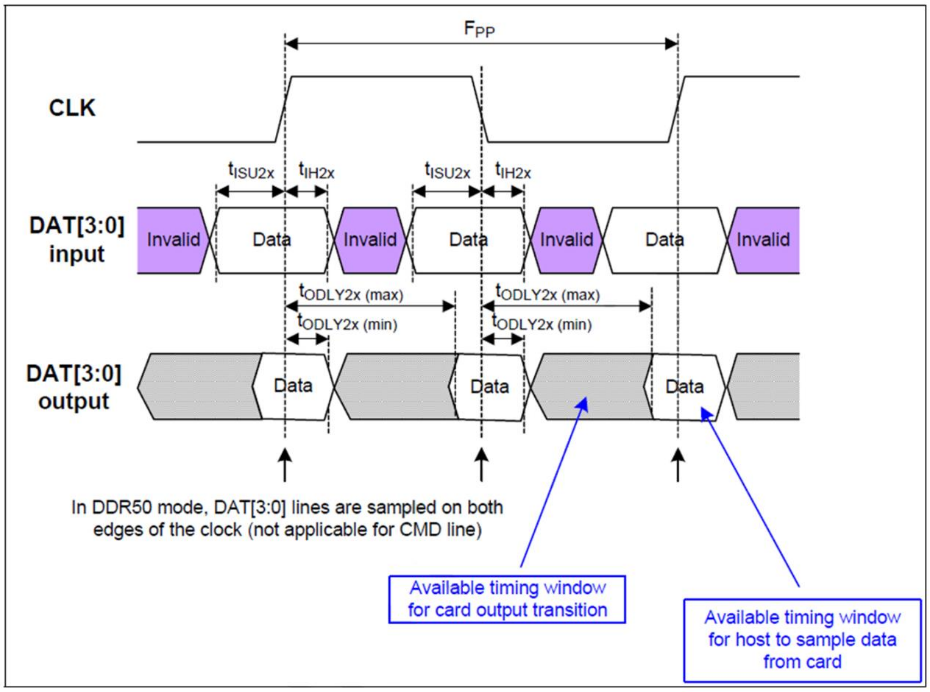

Figure 2-22. MSDC input/output timing diagram of DDR50 speed mode

Table 2-23. MSDC AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	C_L≦30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≧15pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	C_L≦25pF (1 card)
Output hold time	t_{OH}	1.5	-	Ns	C_L≧15pF (1 card)

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2.2.5.6.5 HS200 Speed Timing

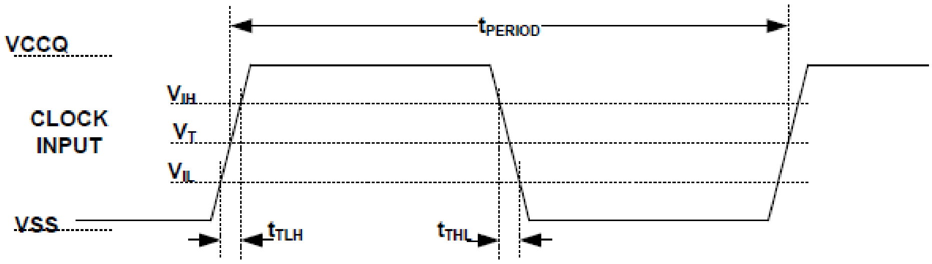
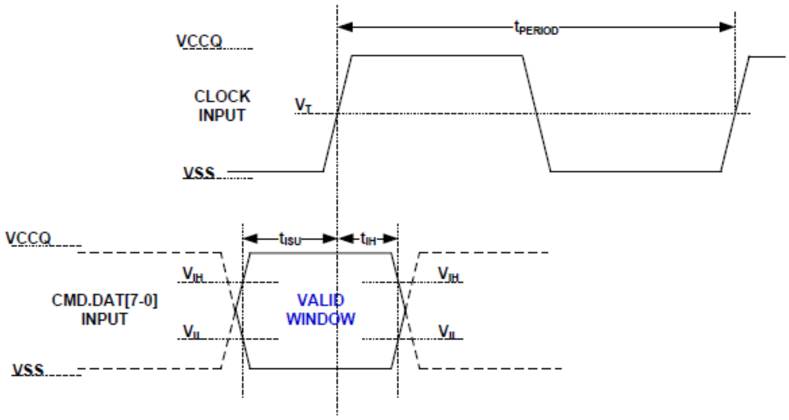


Figure 2-23. MSDC clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-24. MSDC input timing diagram of HS200

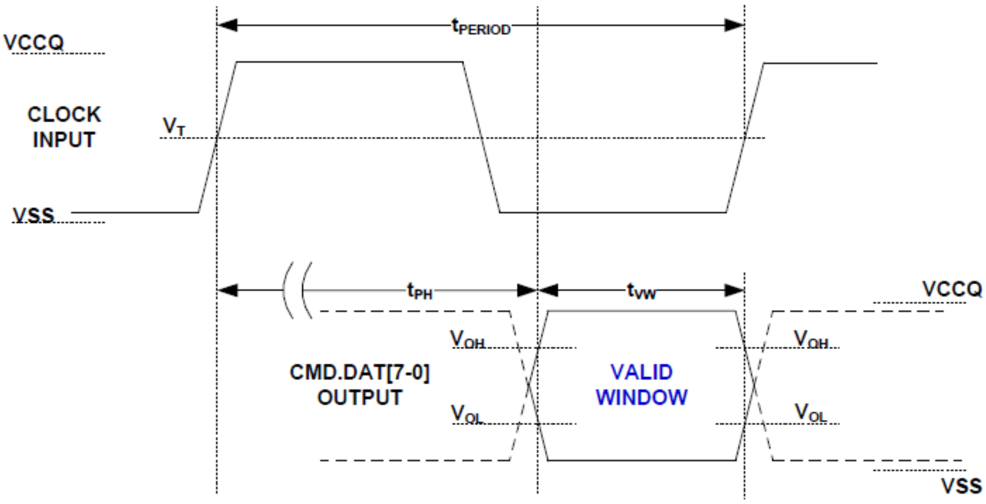


Figure 2-25. MSDC output timing diagram of HS200

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Table 2-24. MSDC AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (max.), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leqq$ 6pF
t_{IH}	0.80		ns	$C_{DEVICE} \leqq$ 6pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay variation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

2.2.5.6.6 HS400 Speed Timing

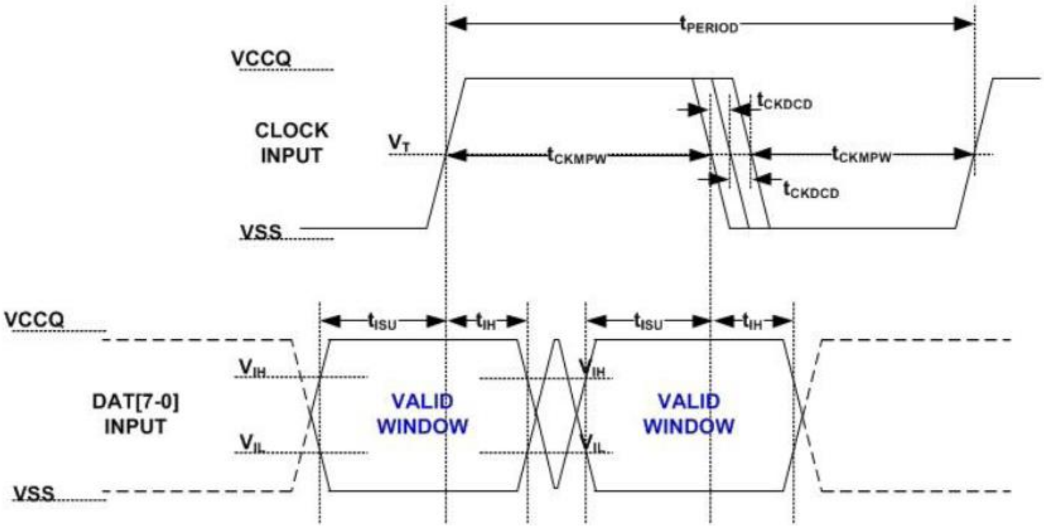

Figure 2-26. MSDC input timing diagram of HS400

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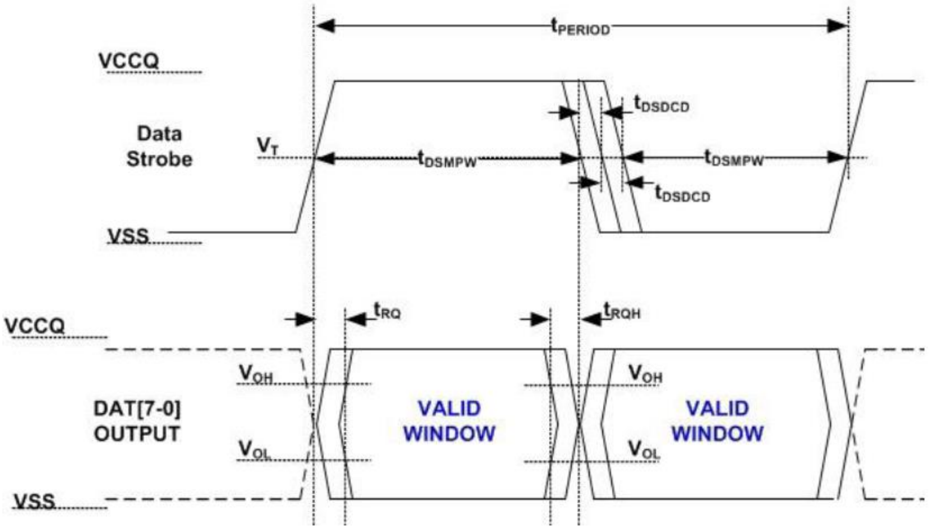

Figure 2-27. MSDC output timing diagram of HS400

Table 2-25. MSDC AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leqq 6$pF. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leqq 6$pF. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.

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Parameter	Symbol	Min.	Max.	Unit	Remark
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.7 SIM AC Timing Characteristics

Table 2-26. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-27. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI0 [1] PWRAP_SPI0_CSN	00: Use SPI pin for legacy JTAG, DPI pin for IO_JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG
[0] AUD_DAT_MISO0	0: NA (default) 1: DP/DM output JTAG
[0] AUD_DAT_MISO1	0: eMMC booting 1: Reserved
[0] PWRAP_SPI0_MI [0] PWRAP_SPI0_MO	00: LPDDR3 01: LPDDR4 10: LPDDR4X 11: LPDDR4X+

2.3.2 Constant Tie Pins

Table 2-28. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence is shown in the following figure:

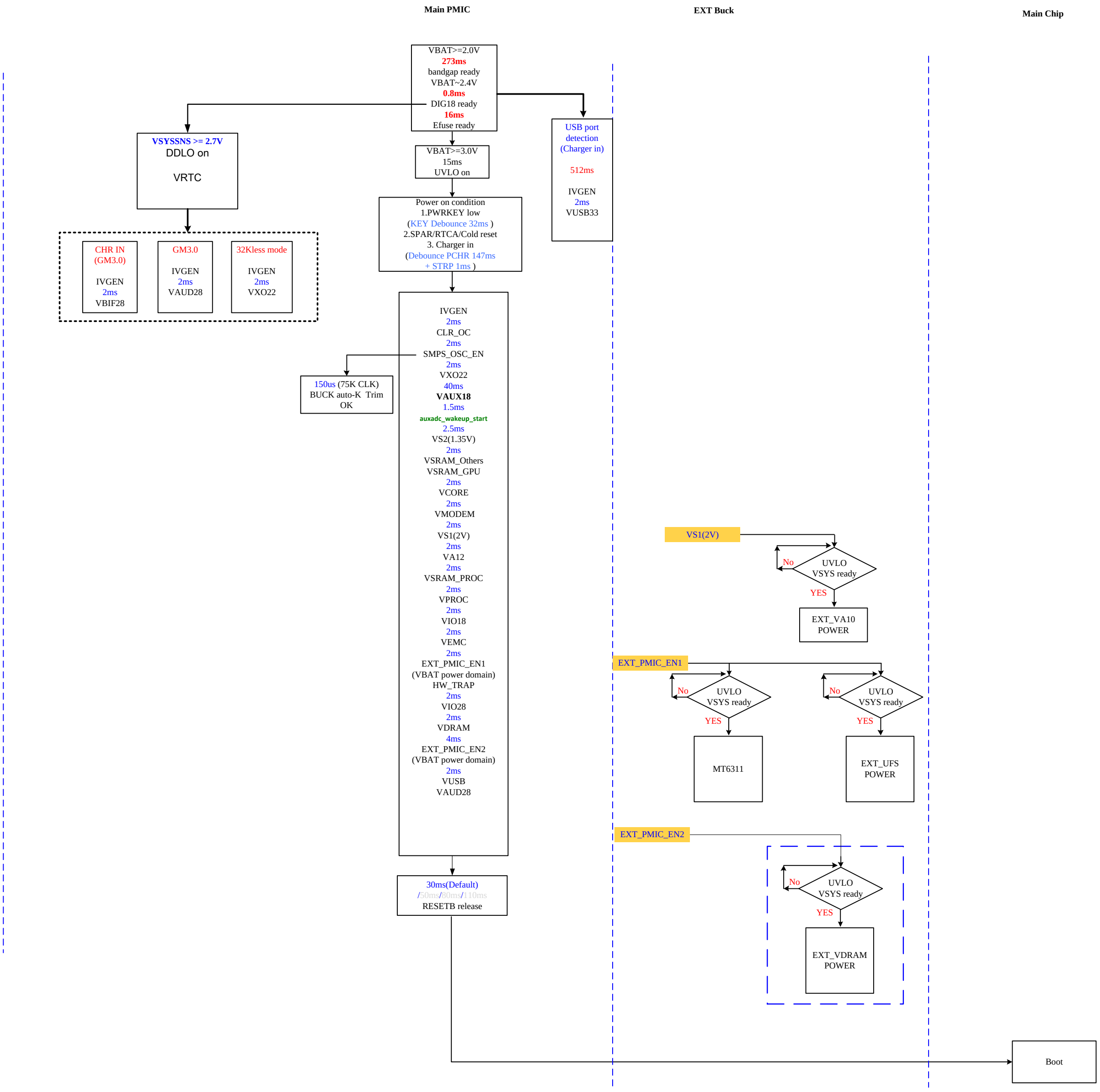

Figure 2-28. Power on sequence

Refer to PMIC datasheet for detailed timing sequence.

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- DETADC: A ADC that detects calibration, thermal data from RF chip.
- RF control: A DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers.
- Auxiliary ADC: Provides an ADC for auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

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1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 8 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

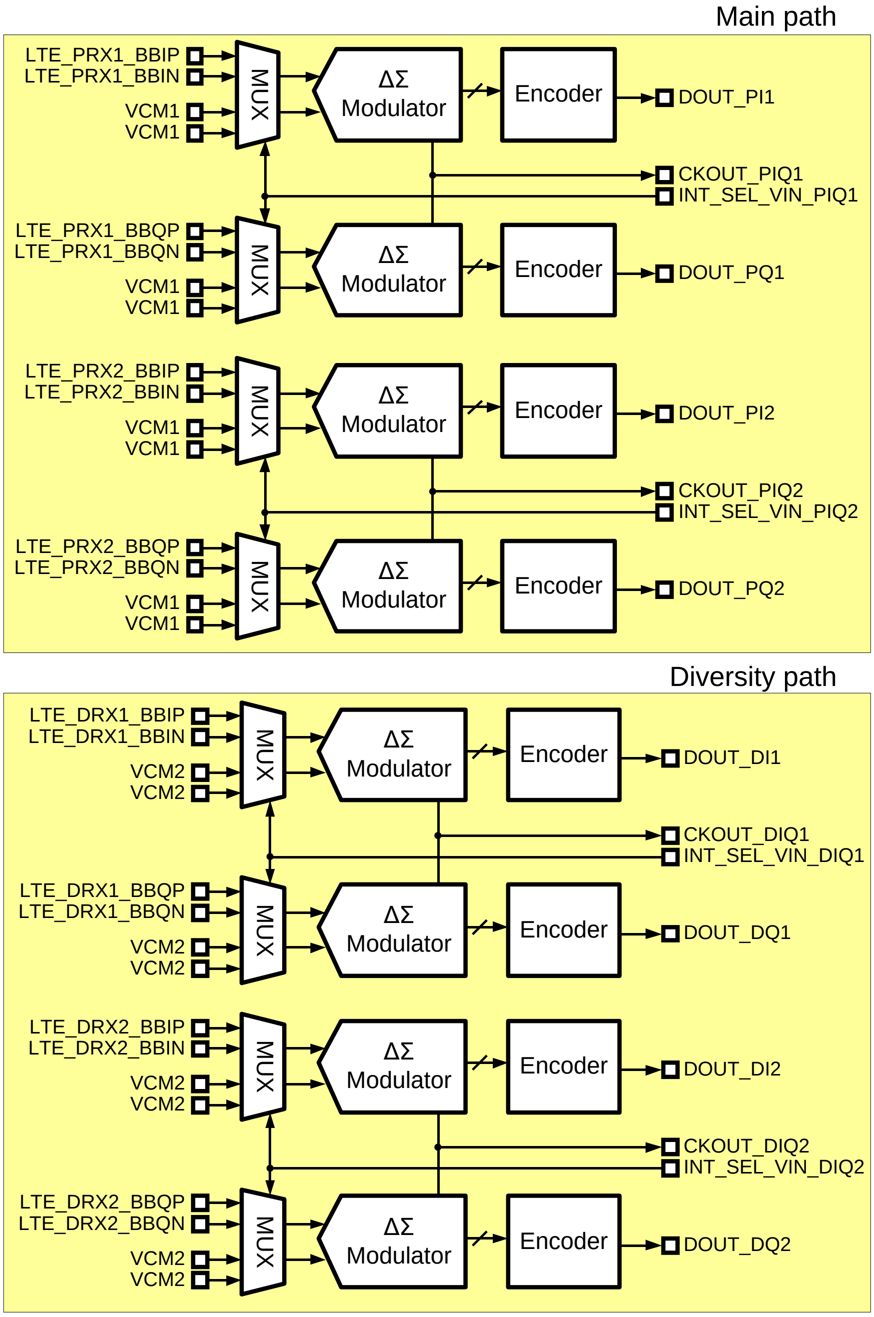

Figure 2-29. Block diagram of BBRX-ADC

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2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-29. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency	208		832	MHz
	Input clock duty cycle	49.5	50	50.5	%
RIN	Differential input resistance	2.8		20.8	kΩ
FS	Output sampling rate	208		832	MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise	70		89	dB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		12.3 10		mA uA

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

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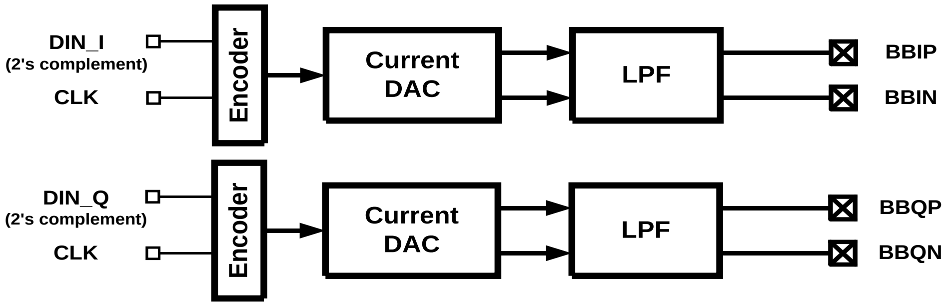

Figure 2-30. Block diagram of BBTX

2.5.3.2.2 Functional Specifications

Table 2-30. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 8 10		 mA uA

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

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1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40MHz 1st-order Butterworth frequency response.

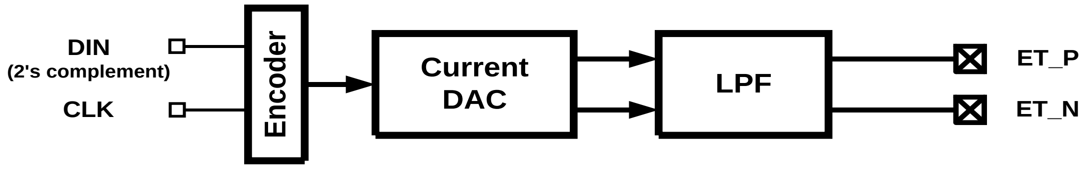

Figure 2-31. Block diagram of ETDAC

2.5.3.3.2 Functional Specfications

Table 2-31. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.
2. 12-bit A/D converters: Converts the detected signals to 12-bit digital data sampled at 104MHz.

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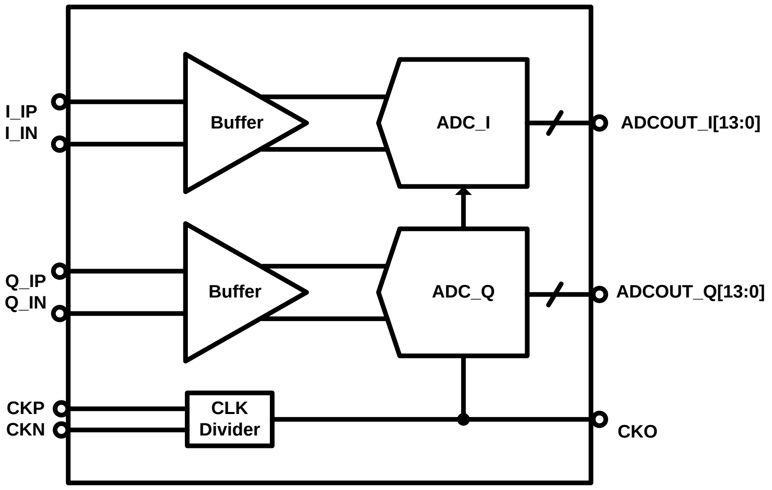

Figure 2-32. Block diagram of DETADC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

Table 2-32. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
FS	Sampling rate		104		MSPS
VOS	Differential input referred offset		30		mV
SNDR	Signal-to-noise-and-distortion ratio		60		dB
DR	Dynamic range		63		dB
THD	Total harmonic distortion		-66		dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 6 1		 mA uA

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2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

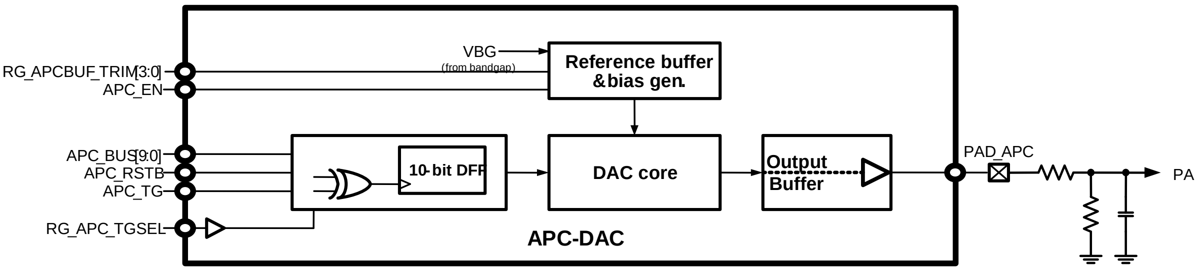

Figure 2-33. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-33. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	−20		85	°C
	Current consumption – Power-up – Power-down		 450 20		 uA uA

2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

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1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-34. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		4/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel (PAD loading excluded)		 50 4		 fF pF
	Clock latency		N+8		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

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Table 2-35. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
	Maximum Positive Overshoot			1.98	V
	Minimum Negative Overshoot	-0.1			V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		650		uA

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-36. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

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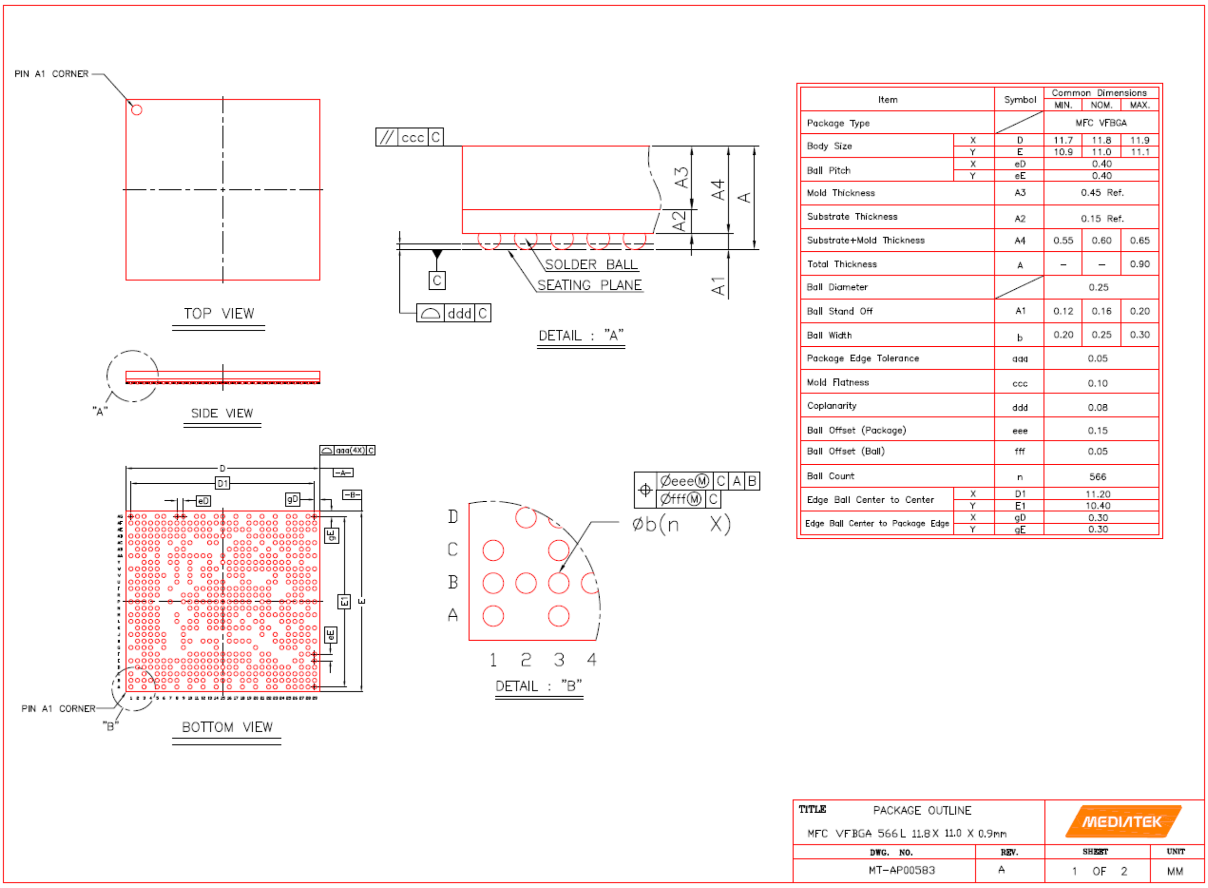
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				MFC VFBGA	
Body Size	X	D	11.7	11.8	11.9
	Y	E	10.9	11.0	11.1
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.45 Ref.	
Substrate Thickness		A2		0.15 Ref.	
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.90
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		566	
Edge Ball Center to Center	X	D1		11.20	
	Y	E1		10.40	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 2-34. Outlines and dimensions of VFBGA 11.8mm*11mm, 566-ball, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 2-37. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	37.65	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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2.6.4 MSL

MSL of this chip is 3.

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2.7 Power Delivery Network

Table 2-38. PDN specifications

Power domain	RDC	RRemote	Frequency range: 0.1~100MHz, equivalent RLC model		
	(mΩ)	(mΩ)	R (mohm)	L (nH)	C (uF)
VPROC	12	1.5	12	0.15	28.5
VMODEM	25.4	3.2	25	0.30	41.0
VGPU	12.0	3.0	25	0.30	44.8
VMD1	12.0	12.9	25	0.30	
VCORE	12.0	3.6	25	0.20	
VEMI_VDD2	40	4	20	0.30	34.2
VEMI_VDDQ	150	15	20	0.30	
VDRAM_VDD2	40	4	20	0.30	
VDRAM_VDDQ	50	5	20	0.30	

Note: Refer to document "MT6763_PDN_Checking_Notice.pdf" on DCC for more design concepts.

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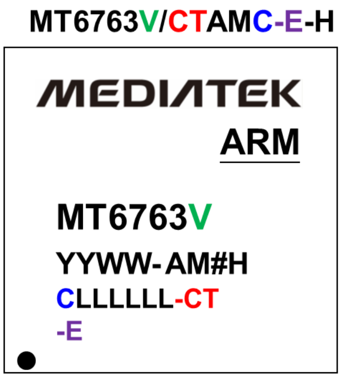
2.8 Ordering Information

2.8.1 Top Marking Definition



- V: Package code
- YYWW: Date code
- CT: Function code
- #: Subcontractor code
- LLLLLLL: Lot number
- E: Eng version

Figure 2-35. Top marking of MT6763

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